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D4 Digital Channel Bank Family:

Thin-Film Dual Active Filter for Pulse Code Modulation Systems

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This article describes the design of a new thin-film dual active filter for pulse code modulation (PCM) systems. A synergistic combination of circuit, silicon, and thin-film innovations has reduced the size, power, and cost of the filter and has expanded its applications. In the latest design, both the band-limiting and reconstruction filters are fabricated on a single ceramic hybrid integrated circuit in a way which significantly reduces their size, power, and cost, along with improving their performance. The filters are fabricated using laser-patterned and laser-trimmed thin-film resistors, a custom-designed complementary bipolar quint operational amplifier (op-amp), and reduced-capacitance circuit design with an innovative interconnection technique. The techniques used to minimize crosstalk between the filter sections are also described and performance data is presented. The evolution of thin-film filters for Bell System PCM systems is also briefly reviewed.

I. INTRODUCTION

The first major Bell System application of resistor-capacitor (RC) active filters was in the D3 channel bank. These filters were fabricated using tantalum thin-film resistors and capacitors[1] and beam-leaded silicon integrated circuit (SIC) operational amplifiers. They have been manufactured since 1971. Evolution of the technology has reduced the cost, size, and power of these filters and has expanded their application to other systems. The filters are currently being used in D3, D4, DCT, *SLC**-96 subscriber loop carrier, LT1, and several other PCM systems. This article briefly reviews the history and application of these filters in PCM systems and describes the latest design: a dual filter fabricated for single in-line package (SIP) mounting.

Most PCM systems that encode and decode a voice-frequency (VF) signal require two filters for each channel. A simplified view of the D4 channel bank is shown in Fig. 1. A filter is required to band limit the signal before it is encoded to avoid aliasing from the 8-kHz sampling rate. This is often called the transmit filter. Another filter, called the receive filter, reconstructs or smooths the output from the decoder. Similar filters are required if per-channel coders-decoders (CODECS) are used.

The typical transmit-end and receive-end four-wire response limits for the transmit and receive filters are shown in Figs. 2 and 3, respectively. Since there are other sources of channel-frequency shaping, somewhat tighter limits are applied to the filters alone. Manufacturing yield is high enough that separate designs for the wider two-wire frequency response limits are not needed. The transmit filter must provide gain, 60-Hz rejection, and proper termination for the hybrid transformer. The receive filter must correct for the sin x/x frequency response of the decoder. (Figure 3 shows the total response of the receive filter, including sampling effects.) The exact amount of correction depends on the decoder and whether a shared or per-channel approach is being used. The receive filter must also properly terminate the hybrid integrated circuit (HIC) and provide enough signal power to the line through the HIC. Both filters must have low-noise and low-distortion levels. For D3 and D4 applications the gain at 1 kHz is held to ± 0.035 dB for each filter to avoid any gain adjustments on the channel unit.

Figure 4 shows how the filters have evolved in the past decade. In the earlier designs the transmit and receive filters were individually packaged. In the latest design the transmit and receive filters are on the same substrate. Innovations in circuit design, silicon integrated circuit design, and thin-film technology have steadily reduced the cost of the filters (in spite of inflation).

The earliest designs[2] used 125-μm minimum thin-film feature size, 100-ohms-per-square resistors adjusted by anodization, a twin-T circuit[3,4] that required two separate tuning procedures, and individual beam-leaded operation amplifiers. Thin-film components were used for frequency compensation of the amplifiers.

In 1977, the circuit size was reduced by using 300-ohms-per-square laser-adjusted thin-film resistors and 50-μm lines realized in a dual in-

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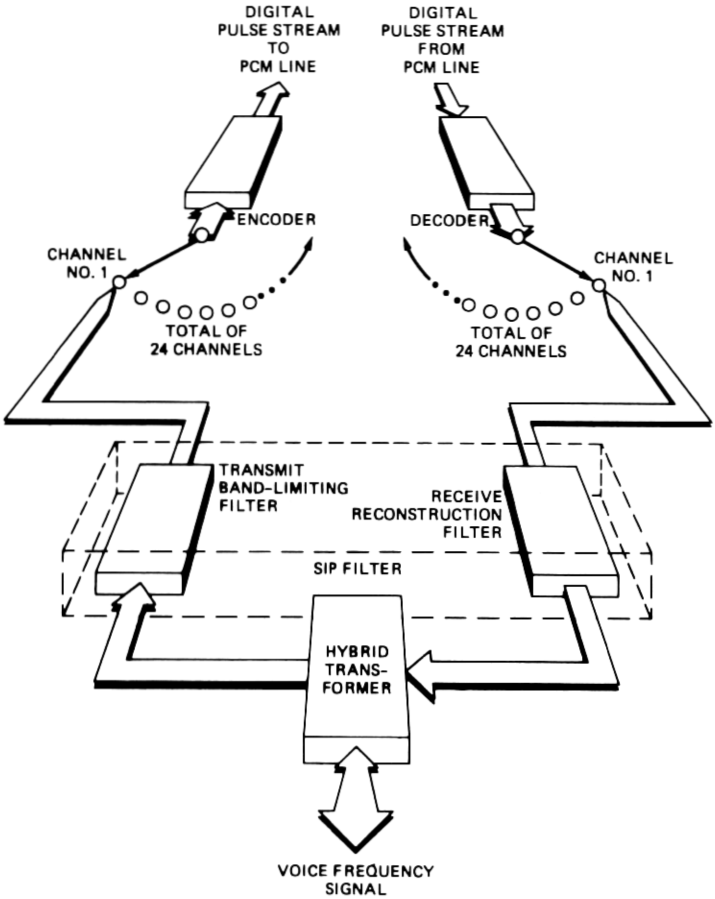


Fig. 1—PCM channel bank.

line package (DIP) format. A lower sensitivity circuit design, improved stability capacitors,[5] and an improved tuning algorithm[6] increased yields and reduced tuning time and cost. The individual beam-leaded operational amplifiers used internal frequency compensation. The same transmit and receive filter film-integrated-circuit layouts were used for all applications. However, they were tuned to somewhat different values for the different applications.

The latest design uses a SIP configuration for vertical mounting and it will be referred to as the SIP filter. Because the transmit and receive filters are packaged together, techniques to reduce crosstalk are required.

Earlier filters have many leads in addition to the few required to connect the filter to other circuits. These are necessary because the tuning procedure requires access to all passive components for mea-

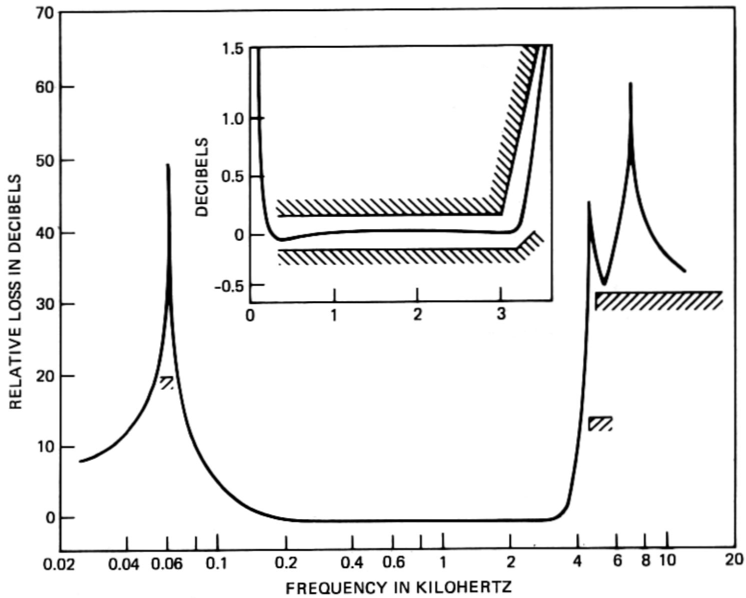


Fig. 2—Transmit filter frequency response.

surement. Some filter-circuit paths must be broken to allow this. The printed-wiring board contains interconnections to complete the filter circuit. Also, each of the four operational amplifiers (op-amps) (two per filter) is an individual SIC. The SIP filter uses a single quint op-amp SIC that consumes 50 percent less power than the four separate op-amps of the earlier designs. When an extra op-amp is installed, a filter circuit with a lower total capacitance can be used. Extra paths on the silicon replace all interconnections formerly provided by the extra HIC leads. Only the functional SIP leads are necessary, which helps size and cost reduction.

The use of a laser-patterned resistor has significantly reduced the size of the filter circuit.[7] Earlier designs used larger photolithographically produced resistor patterns. Also, a "short" RC process involving fewer masks is being used to reduce processing costs even further.[8] A more detailed description of the circuit, silicon, and thin-film design follows.

II. CIRCUIT DESIGN

There are many active filter circuits that can be designed to meet PCM filter requirements. The design must be optimized for the particular manufacturing process being used. Key considerations are parameter values, tuning method, sensitivity, noise, and requirements on

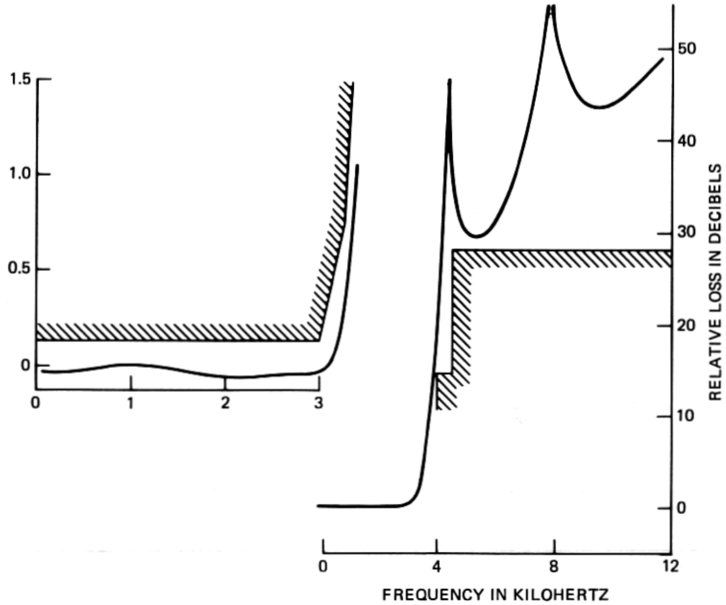


Fig. 3—Receive filter frequency response.

active devices, since these affect size, yields, process time, and performance. To take advantage of the economies of batch processing, the filter circuit size was reduced by reducing total capacitance and improving interconnection strategy.

2.1 Circuit description

Figure 5 is a schematic of the SIP filter. The receive and transmit section are described separately below.

The receive section consists of a four-capacitor input section followed by a second-order notch section. For D4 and similar applications the input signal is a narrow pulse amplitude modulation (PAM) signal from the shared decoder and the demultiplexing junction field-effect transistor (JFET) gate. The demultiplexing gate is switched at an 8-kHz rate. Although the gate is not on the SIP filter, its effect on the filter must be considered in the design. Consequently, the receive filter must be designed as a periodically switched linear network. A switched network analysis program[9] coupled to an optimization routine is used for the design. The optimization procedure determines the parameter values needed to achieve a flat pass band and the desired stop-band rejection with the pulsed input.

In the first section, the JFET demultiplexing gate and the input capacitor approximate a sample and hold operation for the narrow

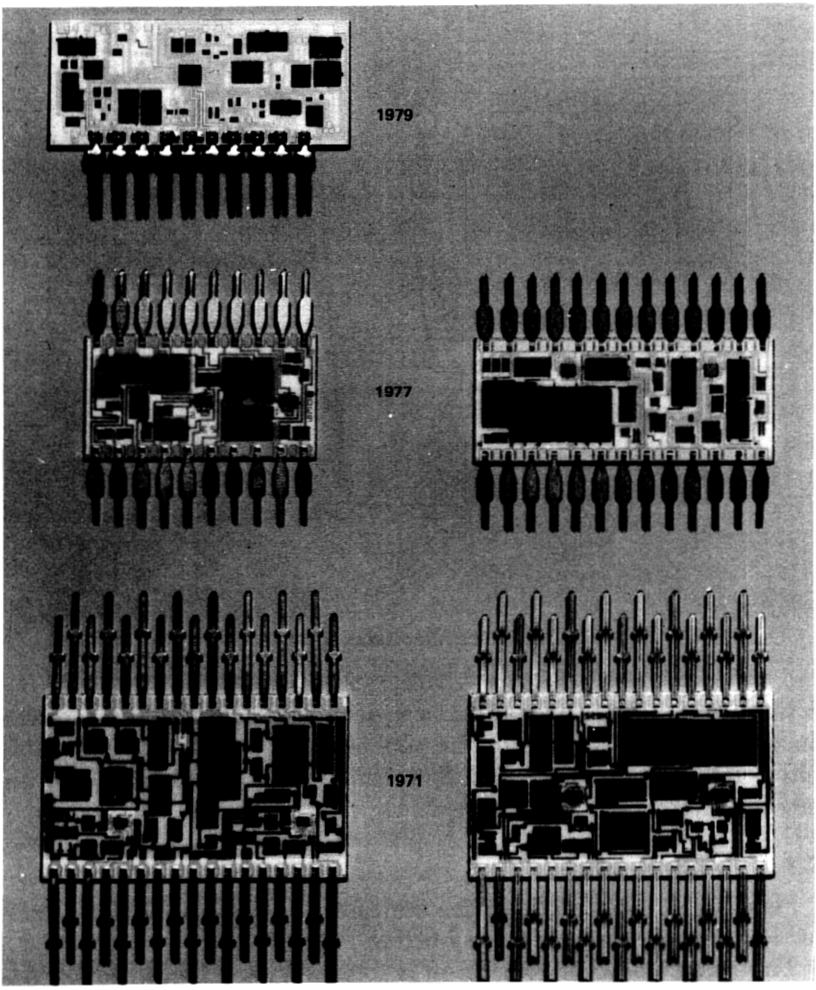


Fig. 4—PCM filter evolution.

PAM input pulses. To minimize effects of variations of JFET device parameters on filter gain, a third-order, low-pass section[10] based upon a second-order Sallen-and-Key low-pass section was chosen to follow the input capacitor. While there is still some interaction between the input capacitor and the third-order stage, this design is less sensitive to JFET device parameters than were previous designs. The second section is a Friend-biquadratic-notch section.[11,12] This section must provide enough power to drive the line through the hybrid transformer and present a proper termination impedance.

The design may be used with per-channel CODECs. In this case the

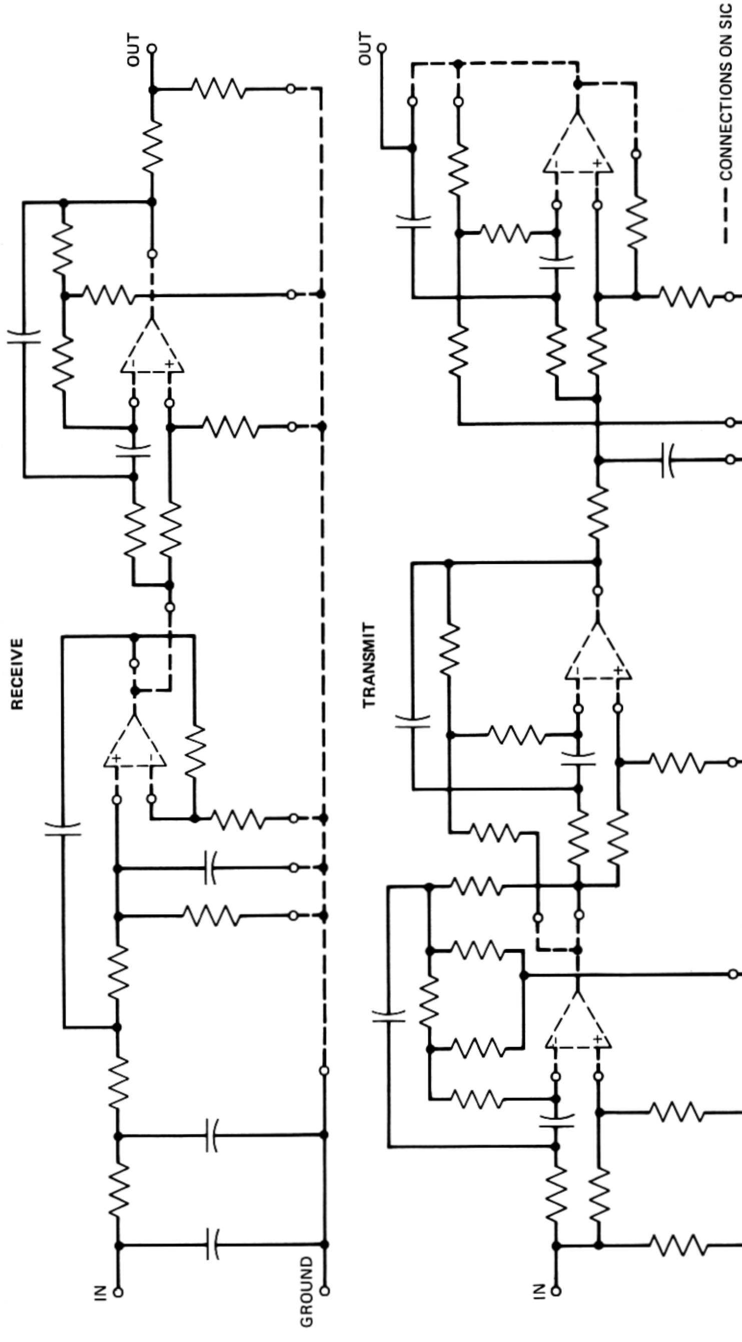


Fig. 5—SIP filter schematic.

input is not sampled but sin x/x frequency-response compensation is still required. The same ceramic circuit can be used if the input capacitor is disconnected (laser scribed open) and slightly different resistor values are used.

The transmit section is a cascade of three Friend-single-amplifier sections. The first section uses additional resistors to reduce the feedback, so-called resistive gain enhancement, and to achieve adequate flat gain. The paralleled input resistor provides proper input termination. A first-order, low-pass RC is combined with a biquadratic notch section to form the third section. The amplifier of the third section must drive the sampling/multiplexing gate preceding the encoder, so adequate settling time with this load must be achieved. The previous transmit design used a fifth-order section to realize a combined third-order, low-frequency, high-pass section and a second-order, higher frequency, low-pass notch. However, although the sensitivity of this stage was adequate, a lower capacitance design could not be achieved without increasing noise. Consequently, a 60-Hz notch section and the low-pass notch are realized as separate sections, requiring an additional op-amp. To further reduce total capacitance below the level of the 1977 design, power supply bypass capacitors are omitted from the HIC.

Pole-zero pairing, section ordering, and gain levels are chosen to minimize noise and achieve adequate dynamic range. The designs are less sensitive to parameter variations than previous designs and tuning is required only to account for passive component tolerances, not for active device parameter variations.

2.2 Tuning and interconnection

In manufacture, capacitors are allowed to vary ±10 percent and resistors must be adjusted to value in the thin-film trimming process. Capacitor variations can be compensated for by measuring capacitors and adjusting resistors to values calculated to achieve the desired transfer function. Alternatively, gain measurements can be used instead of resistor or capacitor measurements. However, resistor and capacitance value measurements can be made faster than gain measurements. As we mentioned in the previous section, tuning to compensate for gain variations because of active device variations is not required in the tuning process.

Individual access is required to measure each resistor and capacitor. However, measurement access is necessary only before silicon attachment. In the SIP filter, the probe pads for measurement access are internal connections rather than edge connections to reduce the size of the layout. The shunting effect of loops of resistors in parallel with a capacitor must be broken to allow measurement of capacitor value and leakage. Loops of resistors are broken to ease resistor measurement. (Three-terminal resistance measurements can be made, but accuracy is reduced.) After tuning the resistors, the broken loops are connected by extra beams and associated metalization provided on the SIC. The connections made on the SIC are shown in Fig. 5. The extra HIC leads and paths required on the printed-wiring board for previous designs to achieve measurement access are eliminated, resulting in substantial size reduction.

To relax resistor-adjustment-accuracy requirements, a mop-up tuning procedure is used.[6] After all capacitor values have been measured, the value of the first resistor to be adjusted is computed and the resistor is laser trimmed. The trimmed value is measured and is used with capacitor values to compute the value of the second resistor to be trimmed. Succeeding resistors are trimmed to values based on capacitor values and values of previously trimmed resistors to minimize the deviation from the desired transfer function. Using this sequential procedure, a substantial portion of the effects of resistor adjustment tolerances can be eliminated and resistor trim tolerances can be loosened.

Most of the circuits require only this parametric tuning. Because of the tight 1-kHz gain requirement, a small fraction of the circuits require an adjustment of a few resistors based on 1-kHz gain measurements made after the silicon is attached.

Somewhat different filter responses are required for the various applications of the SIP filter. These can be achieved with the same circuit if different resistor values are used. The same ceramic-film integrated circuit (FIC) and quint op-amp SIC are used for all applications. The SIP filter is customized at the laser trim stage to tune to the particular response desired using the appropriate tuning data. Significant economies result, since the different applications can use common film processing and common tooling and fixtures.

III. SIC DESIGN

3.1 Requirements

The quint op-amp SIC was custom designed for use on the SIP filter. As mentioned in the previous section, additional metalization on the SIC provides crossovers and tie-points for the HIC to reduce the number of HIC leads. With transmit and receive filters on the same HIC, cross talk is a concern, so techniques to minimize it are incorporated into the design. By sharing common circuits in the op-amp current supply and by designing peak current capability for each amplifier only as needed, a power savings is achieved. Short-circuit protection is needed only for the output amplifier of the transmit filter section. A power-shutdown option is also provided. Universal application requires operation from ±4.75V to ±12.6V and allows for a ±16V over-voltage condition. Because of the wide bandwidth of the complementary bipolar process, on-SIC single-pole compensation achieves stability with adequate gain.

3.2 Circuit

Figure 6 shows a quint op-amp circuit diagram. There are three op-amps for the transmit section and two for the receive section. There is a current source for each section and a voltage-reference and power-shutdown circuit serving the entire SIC.

The three stages of each amplifier are of simple design, made possible by the complementary bipolar integrated circuit (CBIC) technology. This technology provides high-quality pnp transistors with β and f_T similar to npn transistors on the same SIC. Dominant pole compensation brings about a 6-dB/octave gain characteristic throughout and beyond voiceband. The approximate total voltage gain can be shown to be

$$A_{\text{VOL}} \approx \frac{w_T}{w},$$

where

$$w_T = \frac{I_{inp}}{2V_T C}, \quad V_T = \frac{kT}{q}.$$

I_{inp} is the total input stage current and C is the compensation capacitance. The adjustment of I_{inp} and C, within the restraint of a minimum A_{VOL}, is made to accommodate the desired noise performance and low-frequency voltage gain, to allow a reasonable compensation capacitor size, and to ensure adequate gain and phase margins at high frequencies. The resistor in series with the compensation capacitor puts a zero in the transmission characteristic to compensate for a second pole near 15 MHz.

Only the output amplifier of the transmit section is directly connected to an external lead. The other amplifiers have some circuit resistance in series to limit output current. Short-circuit protection for the output amplifier of the transmit section is provided in the standard manner.

Each filter section is powered from a separate +V supply. There is a common −V supply that is tied to the SIC substrate. To minimize cross talk, separate transmit-section and receive-section current sources are used from a common zener reference. There is a "current-mirror" circuit in the receive-section current source that guarantees, even at low-supply voltage, a minimum zener-diode current of about

200 μA to eliminate microplasma noise. The shunt resistor across the "current-mirror" circuit is used for startup. The power-shutdown circuit diverts current from the zener diode when the power-down lead is high [transistor-transistor logic (TTL) levels]. This turns off the current sources to disable the amplifiers.

3.3 SIC layout

A total of 20 beams is required to provide the op-amp circuit functions of the SIC. An additional 15 beams are required for crossovers and tie points. A 36-beam SIC has enough area for devices and for the additional metalization paths. The SIC layout is shown in Fig. 7. Superimposed on the SIC is an outline dividing the area according to function.

Electrical isolation between the transmit and receive sides of the SIC minimizes crosstalk. To assure electrical isolation the transmit and the receive amplifiers occupy separate epitaxial tubs isolated from each other by a region biased at the substrate potential. Separate positive supplies bias the epitaxial tubs with respect to the substrate. Also, the positive and negative power supply, the current sources, and the power shutdown circuitry are placed between the transmit and receive op-amps.

Power dissipated in the output transistors creates a thermal gradient across the SIC. The output stage of each op-amp is a Class AB complementary-emitter follower. Of particular concern is a change in the thermal gradient as power switches between the output transistors. Thermal gradients affect offset voltages of the op-amp input transistors so that changes can result in thermal feedback and thermal crosstalk between receive and transmit amplifiers at low frequencies. A thermal-analysis computer program was used to plan the SIC layout.

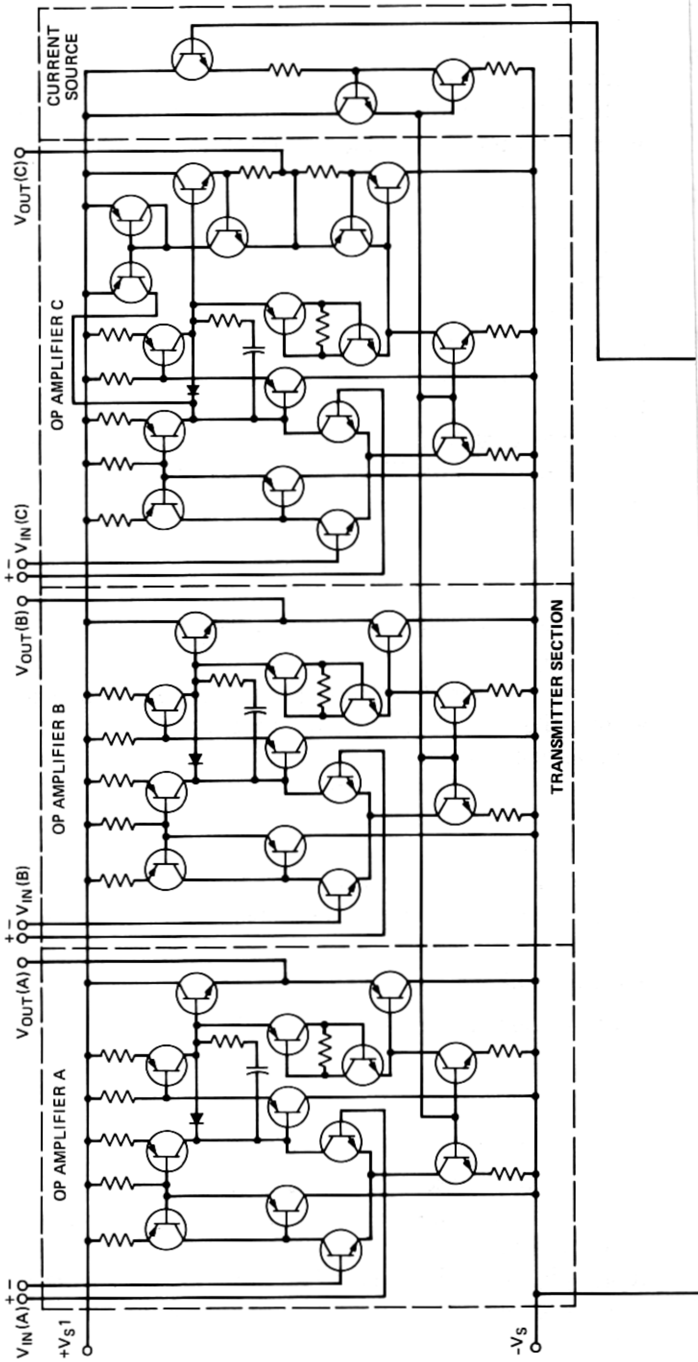
3.4 Performance

Table I lists important measured amplifier parameters.

IV. HIC DESIGN

4.1 Laser-patterned resistor

A new laser-patterned resistor was developed[7] to take advantage of the smaller feature size achievable with laser machining. Line and space widths smaller than those practical with off-contact photolithography are achievable. The new resistor has the high stability of conventionally patterned resistors and is compatible with standard RC processes. Also, for most values, the resistor is significantly smaller than conventional resistors.


CURRENT SOURCE
V_OUT(C)
OP AMPLIFIER C
+ − V_IN(C)
V_OUT(B)
OP AMPLIFIER B
+ − V_IN(B)
V_OUT(A)
OP AMPLIFIER A
+ − V_IN(A)
+V_S1
−V_S
TRANSMITTER SECTION

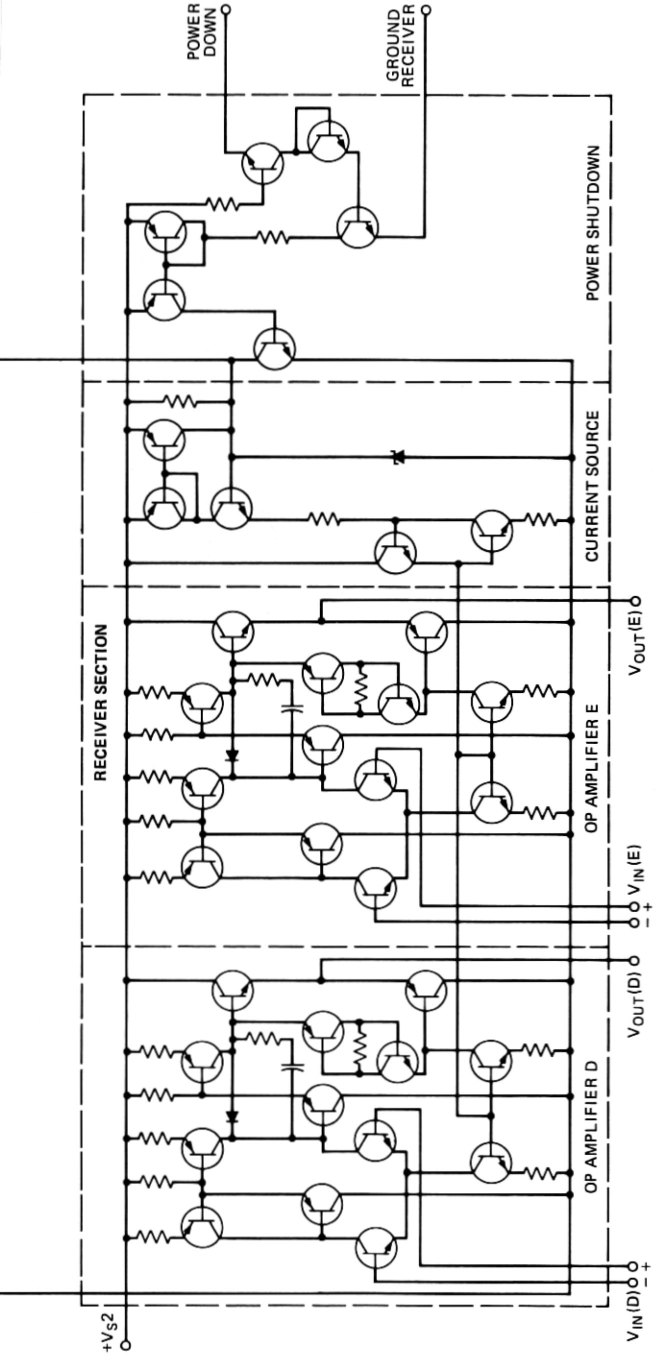


Fig. 6—Quint op-amp circuit diagram.

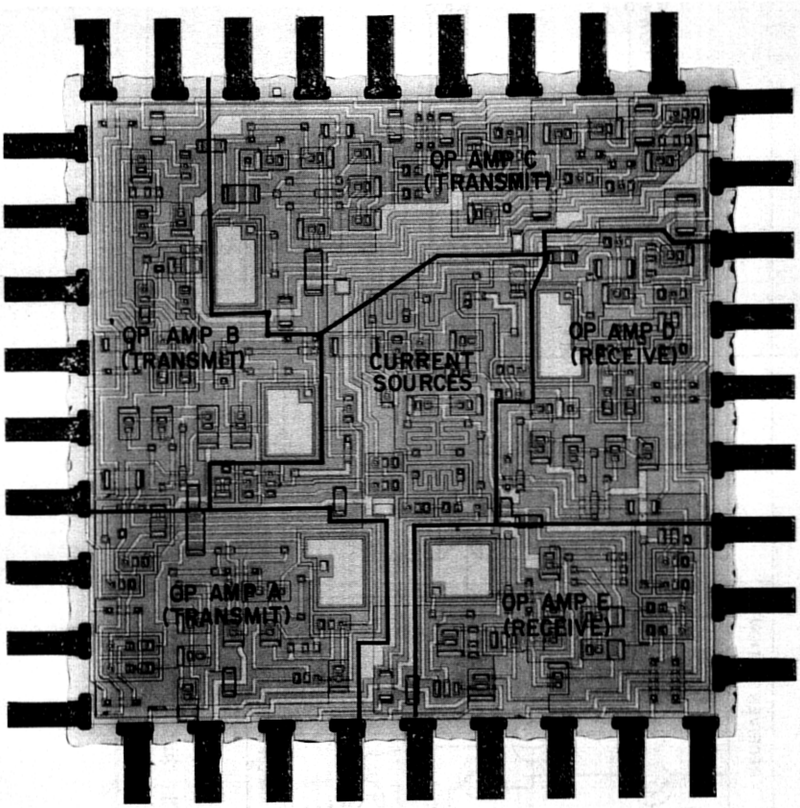


Fig. 7—Quint op-amp.

Figure 8 shows a typical laser-trimmed resistor from a standard library. The pattern is etched using standard off-contact photolithography. In the 1977 filter designs, 50-μm minimum line and space widths are used on 300-ohms-per-square Ta_2N film. The resistors are adjusted

Table I—Typical amplifier characteristics

Unity gain frequency		4.5 MHz
Phase margin		70 degrees
Power	±6V	33 mW (on)
		4.6 mW (off)
	±12V	63 mW (on)
		8.1 mW (off)
Power supply rejection ratio		3 $\mu V/V$
Isolation (Transmit to receive or receive to transmit)	$V_{in}^{T,R}/V_{out}^{R,T}$	≤−130 dB
Noise (Input referred, R_{in} = 1K)	C-message	0.63 μV (rms)
	3-kHz Flat	0.75 μV (rms)
$\Delta A_{VOL}/\Delta V_S$		−0.05 dB/volt (supply)
$\Delta A_{VOL}/\Delta T$		−0.02 dB/°C

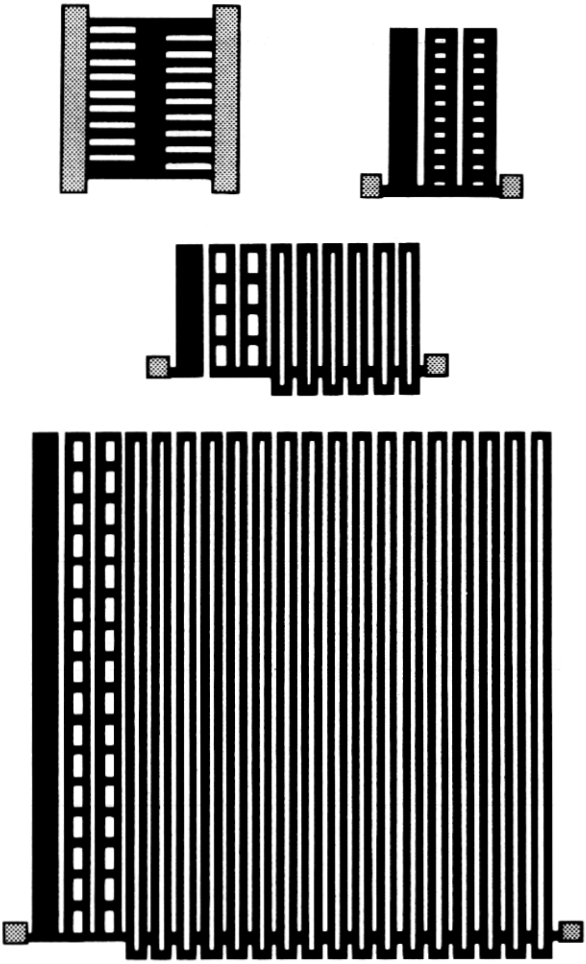


Fig. 8—Typical standard library laser-trimmed resistor.

to value by first scribing open "loop" or "ladder" shunt connections. Final adjustment is made by a continuous-beam laser trim.[13]

Figure 9 shows the design of the new laser-patterned resistor. To minimize resistance drift after laser machining, a wide-space pattern is cut after the narrow-space pattern. The process begins on a rectangular block of thermally stabilized 300-ohms-per-square Ta_2N film. About 90 percent of total resistance is realized using a laser-machined serpentine pattern of 25-μm line and space widths followed by cleaning and thermal stabilization. About a four-percent change in resistance is experienced because of the stabilization of the heat-affected zone contiguous to the laser-cut region. The resistor is now about 94 percent

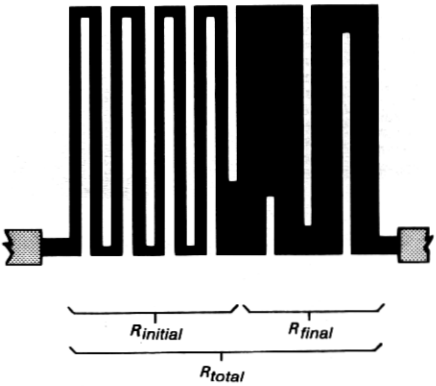


Fig. 9—Laser-patterned resistor.

of the desired value. The remaining adjustment (about six percent of total resistance) is achieved using 100-μm spacing of 25-μm laser cuts. This two-width procedure achieves resistor stability equal to conventional resistors.

In Figure 10 the areas required for the laser-patterned resistor and conventional resistor are compared. Savings of a factor of 1.5 for high values (700 kilohms) to 5 for low values (<5 kilohms) are evident.

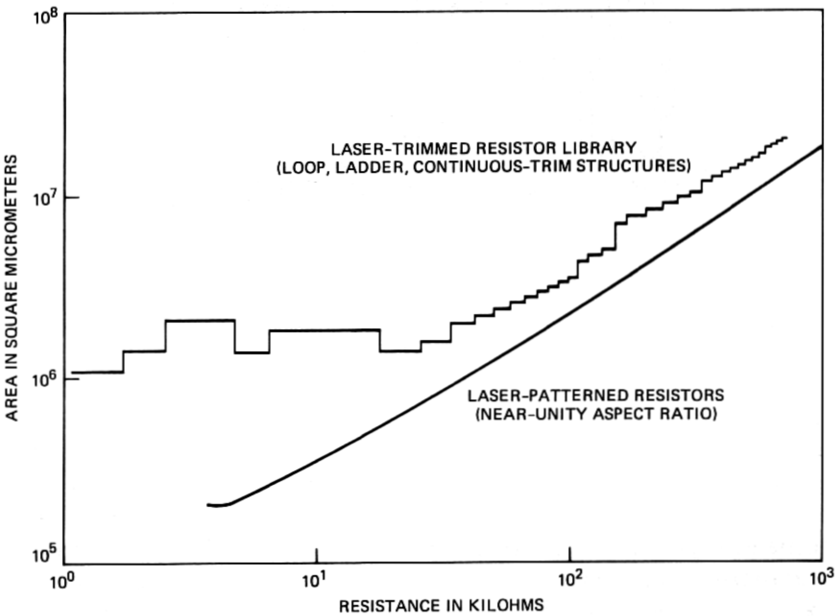


Fig. 10—Comparison of resistor areas.

4.2 Layout

Figure 11 shows the HIC with the quint op-amp mounted and leads attached, but without encapsulation applied. As previously mentioned, a large size reduction was achieved by reducing total circuit capacitance, and by using interior probe points, the laser-patterned resistor and SIC beams and metalization for tie points and crossovers. These allowed both transmit and receive sections to be realized on a single substrate equal to the size of just the previous transmit filter HIC.

Since only ten external leads are required, a single in-line package (SIP) format can be used to reduce the printed-wiring-board footprint. A new lead was designed for SIP mounting. Extensive shock and vibration evaluations were performed to verify mechanical integrity and stability of proposed and final lead designs. For a few applications, height restrictions preclude SIP mounting. Provision is made for two additional leads to be attached to the corners of the side opposite the functional leads. Instead of SIP leads, DIP leads are used and two additional DIP leads are attached to these opposite corners of the HIC to allow horizontal mounting.

To minimize crosstalk between transmit and receive sections, the most sensitive circuit nodes were identified and were separated as much as possible from high-signal amplitude nodes. A wide path, connected to −V, bisects the circuit to provide an electrostatic shield separating transmit and receive sections.

V. PERFORMANCE

Table II summarizes the important SIP-filter characteristics. The composite characteristics of the two 1977 designs are also listed for

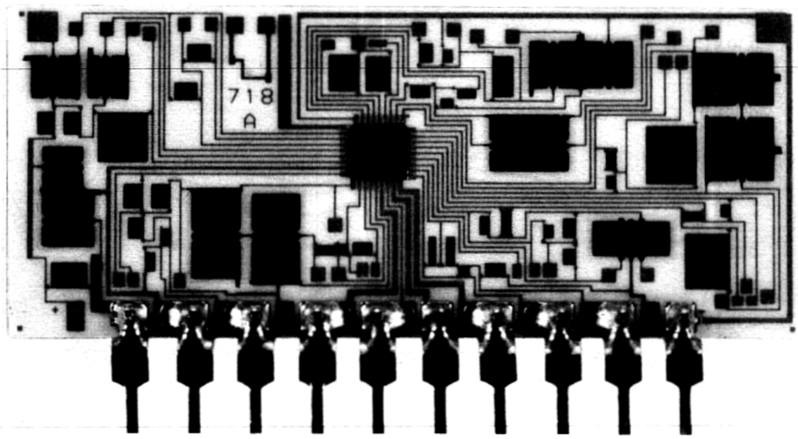


Fig. 11—SIP filter.

Table II—SIP filter performance

		1977 Design	SIP
ΣR		1.7 × 10^6 ohms	1.9 × 10^6 ohms
ΣC	Circuit	47 nF	24 nF
	Bypass	19 nF	0
Power	±12V	120 mW	63 mW
	±5V	—	30 mW
Size		0.6- by 1-in DIP 0.6- by 1.3-in DIP	0.6- by 1.3-in SIP
Distortion (typ) (1 kHz, 3 dBm0)		<−60 dB	<−60 dB
Noise (Output)	Receive	<0 dBrnC	<−1 dBrnC
	Transmit	<8 dBrn (15-kHz flat)	< 4 dBrn (15-kHz flat)
1 kHz gain		±0.035 dB	±0.035 dB

comparison. Figure 12 is a plot of measurements of the transmit portion of a sample of 50 SIP filters. The MIN, MEAN, and MAX lines are the minimum, mean, and maximum, respectively, of the ensemble of loss measurements. They do not necessarily represent the response of any one sample. Figure 13 plots the crosstalk performance between transmit and receive sections, referenced to equi-level points in the D4 channel unit. (For D4, the level at the input to the transmit section is 12.5 dB lower than the level at the output of the receive section.) Also plotted is the D4 channel-unit requirement, showing that the contribution from the SIP filter is not significant.

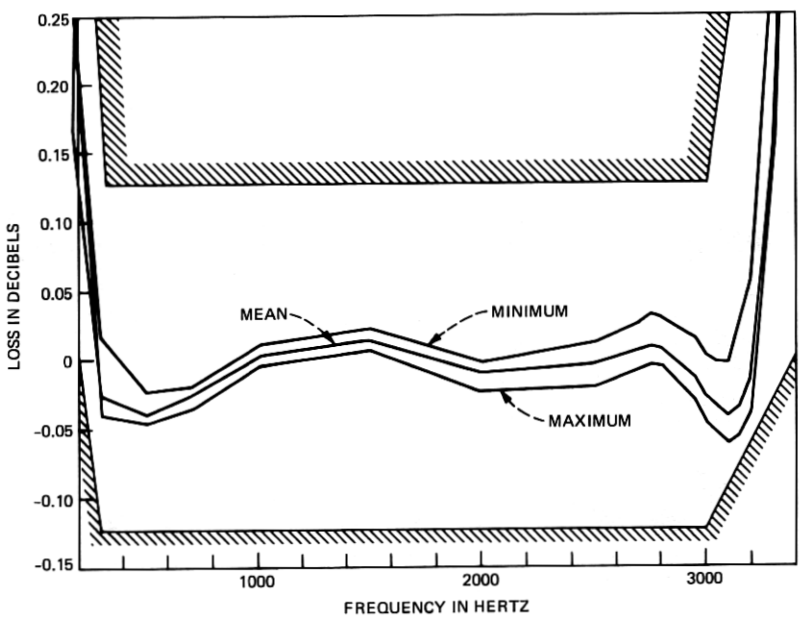


Fig. 12—Ensemble characteristics of measured SIP transmit sections.

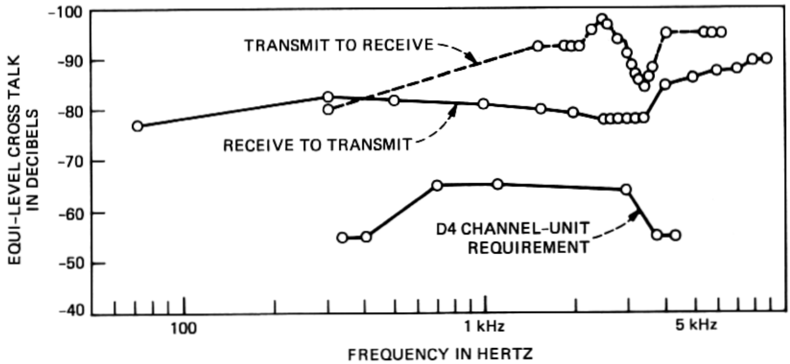


Fig. 13—SIP filter crosstalk performance.

These results, supported by extensive Monte-Carlo analysis and by high-volume production results, show that the SIP filter easily meets *D*-type channel bank requirements.

VI. SUMMARY

The design and performance of a new dual thin-film active filter for PCM channel banks has been described. Synergistic-circuit, thin-film, and silicon technology innovations have resulted in significant size, power, and cost reductions with performance improvements.

VII. ACKNOWLEDGMENTS

Many engineers contributed to the success of the design of this filter. We would particularly like to acknowledge F. J. Witt for his leadership, E. D. Finch for circuit design, L. E. Trego, L. J. Kiszka, and P. L. Scarff for thin-film design, L. D. Heck for silicon design, and M. M. Borek for silicon layout.

REFERENCES

1. W. H. Orr et al., "Integrated Tantalum Film RC Circuits," Proc. 20th Elec. Components Conf. (May 1970), pp. 602–12.
2. R. A. Friedenson et al., "RC Active Filters for the D3 Channel Bank," B.S.T.J., *54*, No. 3 (March 1975), pp. 507–29.
3. G. S. Moschytz, "FEN Design Using Tantalum and Silicon Integrated Circuits," Proc. IEEE, *58* (April 1970), pp. 550–6.
4. G. S. Moschytz and W. Thelen, "Design of Hybrid Integrated Circuit Building Blocks," IEEE J. Solid State Circuits, *SC-5*, No. 2 (June 1970), pp. 99–107.
5. O. J. Duff et al., "A High Stability RC Circuit Using High Nitrogen Doped Tantalum," Proc. 28th Elec Components Conf. (April 1978), pp. 229–33.
6. P. V. Lopresti, "Optimum Design of Linear Tuning Algorithms," IEEE Trans. CAS, *CAS-25*, No. 3 (March 1977), pp. 144–51.
7. P. L. Scarff and L. J. Kiszka, "Laser-Patterned Ta_2N Resistors for Thin-Film Circuits," Proc. 1981 Elec. Components Conf., May 11 to 13, 1981, pp. 449–55.
8. F. R. Arcidiacono, O. J. Duff, and G. J. Koerckel, "A Method of Reducing Cost in the Production of High Stability Thin-Film RC Networks," IEEE Trans. on

Components, Hybrids, and Manufacturing Technology, *CHMT-3*, No. 4 (December 1980), pp. 492–9.
9. M. L. Liou, "Exact Analysis of Linear Circuits Containing Periodically Operated Switches and Applications," IEEE Trans. Circuit Theory, *CT-19*, No. 2 (March 1972), pp. 146–54.
10. G. S. Moschytz, *Linear Integrated Networks: Design*, New York: Van Nostrand Reinhold Co., 1975, p. 251.
11. J. J. Friend, "A Single Operational Amplifier Biquadratic Filter Section," 1970 International Symposium on Circuit Theory, December 14 to 16, 1970.
12. J. J. Friend, C. A. Harris, and D. Hilberman, "STAR: An Active Biquadratic Filter Section," IEEE Trans. CAS, *CAS-22*, No. 2 (February 1975), pp. 115–21.
13. G. A. Bulger, B. A. Unger, and W. H. D'Zio, "Design and Characterization of a Thin-Film Laser Trimmable Resistor and Its Application in RC Active Filters," Proc. Nat. Elec. Conf., 1977, pp. 308–12.