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InGaAsP LEDs for 1.3-μm Optical Transmission

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High-radiance InGaAsP double heterostructure light-emitting diodes (LEDs) that are fast and reliable have been developed for 1.3-μm optical transmission applications. These devices are prepared by liquid phase epitaxy on InP substrates. Improved growth procedures result in large-area wafers (up to 5.4 cm^2) with excellent uniformity and high device yields. Optical power of ~120 μW can be launched into 0.29-NA, 62.5-μm core fiber. On the basis of accelerated reliability tests the median life of these InGaAsP LEDs is expected to exceed 4 × 10^6 h at 70°C and current densities up to 40 kA/cm^2. The projected failure rate owing to output power degradation (−1 dB) is below 1 FIT. These devices are expected to be useful in lightwave systems operating at data rates ≤140 Mb/s.

I. INTRODUCTION

The present generation of optical transmission systems employs GaAlAs laser emitters operating at 0.8 to 0.9 μm.[1] In this wavelength range fiber attenuation (about 4 dB/km) and especially chromatic dispersion limit the usefulness of light-emitting diodes (LEDs) to short data links of few kilometers. By shifting the LED emission wavelength close to 1.3 μm two properties of the fused silica fiber permit much longer distances and higher data rates. First, the fiber loss is greatly reduced at longer wavelength,[2] with cabled fiber loss below 1 dB/km possible. Second, pulse spreading owing to material dispersion is reduced as $d^2n/d\lambda^2$ of the refractive index approaches zero at 1.27 to 1.30 μm.[3] Thus, 1.3-μm LED-based transmission systems with high

data rates and repeater distances in excess of 10 km are feasible.[4] Indeed, transmission experiments have demonstrated repeaterless LED-based operation over a distance of 24 km at the DS3 rate (44.7 Mb/s) and 7 km at rates as high as DS4 (274 Mb/s).[5] Such LED systems are attractive alternatives to laser systems since light-emitting diodes operate over a wide temperature range with unequalled reliability and their drive electronics is very simple.

These advantages of longer wavelength operation can be realized for devices fabricated out of the quaternary alloy $In_{1-x}Ga_xAs_yP_{1-y}$.[6] These alloys can be grown exactly lattice-matched to InP substrates (for $y/x \approx 2.2$) with compositions ranging from 1.1 μm to 1.65 μm.[7] These quaternary LEDs are efficient, fast, and very reliable.[8–11] In addition, very sensitive InGaAsP detectors have been demonstrated,[12] offering a possibility of a common material technology for both emitting and receiving devices.

In this paper we describe the development of state of the art InGaAsP LEDs for optical transmission applications. The paper is divided into six sections. Following the introduction, Section II describes material preparation procedures leading to double-heterostructure wafers with a large area and high quality. Device fabrication is discussed in Section III, with particular attention devoted to large-scale fabrication techniques. In these two sections a description of general procedures is followed by more detailed descriptions of some of the more challenging problems. LED performance in terms of power launched into fibers, speed, and temperature characteristics is discussed in Section IV. Section V describes accelerated aging tests and reliability estimates. These results are discussed and summarized in Section VI.

II. MATERIAL PREPARATION

Double heterostructure wafers, from 1 cm^2 to 5.4 cm^2 in area, are grown in a multiple-well, graphite boat using a two-phase growth technique.[7] InP substrates are polished to an optically smooth finish with a ~1-percent bromine-methanol solution. All the melts used are first equilibrated at 675°C for 16 hours in a H_2 ambient and then quenched. These prehomogenized melts, containing excess InP and Sn dopant where applicable, are then placed in the liquid phase epitaxy (LPE) boat and again equilibrated at 675°C for an additional hour, as schematically shown in Fig. 1. Zinc is added prior to this final equilibration step. During this warm-up and melt homogenization cycle the thermal decomposition of the substrate is minimized by either a cover piece or phosphorus vapor.[13]

Prior to the growth of the first epitaxial InP layer at 650°C, the substrate is subjected to a shallow In etch, which removes about 5 μm

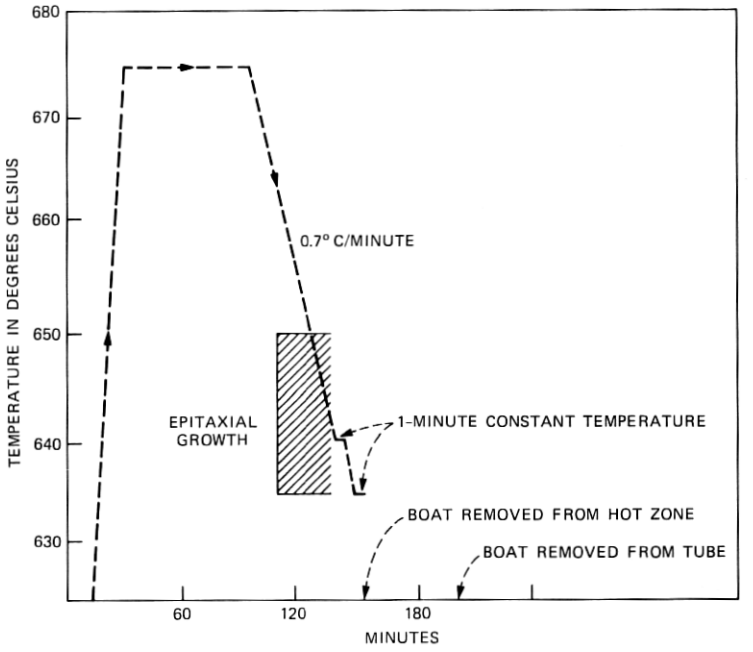

Fig. 1—Schematic diagram of melt homogenization and LPE growth cycle.

of the thermally degraded material. Following the growth of the Sn-doped InP buffer layer at a cooling rate of 0.7°C/min, a nominally undoped quaternary layer is grown isothermally at 640°C. Next, a Zn-doped InP confining layer is grown (again at 0.7°C/min), followed by a Zn-doped quaternary, or the InGaAs ternary, contact layer grown isothermally at 630°C. The InP buffer and confining layers are approximately 5 and 2 μm thick, respectively. The thickness of the InGaAsP active layer is varied between 0.5 and 1.4 μm, while the contact layer thickness is kept at ~0.5 μm.

Since the defects present in the substrate or epitaxial layer are reproduced in the next epitaxial layer,[14] substrate quality is of great importance. InP substrates used in this work have been cut in the ⟨100⟩ direction from the ⟨111⟩ pulled, twin-free, boules grown by the Liquid Encapsulated Czochralski (LEC) technique.[15] The substrates are doped n-type with either Sn or S up to the doping level of $\sim 5 \times 10^{18}$ cm^{-3}. The sulfur-doped material is preferred for reasons of superior macroscopic perfection and higher resistance to thermal damage.[16] The dislocation density in our S-doped wafers, as established by etch pitting and TCL,[17] is typically below 5×10^3 cm^{-3}, as much as an order of magnitude less than in Sn-doped wafers. This reduction has been attributed to lattice hardening.[18] Although the presence of threading

dislocations has been shown to greatly degrade reliability of GaAlAs LEDs,[19] we show in Section V that dislocation density has no significant effect on quaternary reliability. The influence of dislocations on device performance remains to be investigated.

The thermal damage to InP substrate prior to growth and the resulting damage to iso-epitaxial layers are by now well recognized.[20] The damage owing to loss of phosphorus ranges from the large dissociation pits to increased density of phosphorus vacancy-impurity complexes in InP layers,[13] and results in reduced device performance and yield. A number of techniques have been developed to control and eliminate the thermal decomposition, all attempting to provide phosphorus overpressure in the vicinity of the substrate. Commonly used are cover-piece protection,[8] In-Sn-P solution,[21] addition of PH_3,[22,23] or elemental phosphorus at elevated temperature to the growth ambient.[13] Deep, ~25-μm, In meltback also has been used to remove all the degraded material. We have evaluated these protection measures by means of spatially resolved photoluminescence and demonstrated that thermal degradation is present even on morphologically perfect surfaces.[20] A photoluminescence image of a thermally degraded substrate is shown in Fig. 2a. The damage manifests itself as spots of low luminescence efficiency. Iso-epitaxial layers grown on such a substrate show similar damaged regions and an increased dislocation density. This damage depends on the substrate dopant, and is greatly reduced, as indicated by photoluminescence (PL) intensity measurements, in S-doped InP, as compared to Sn-doped wafers. Elimination of thermal damage is achieved through a shallow, ~5-μm deep, In meltback of a

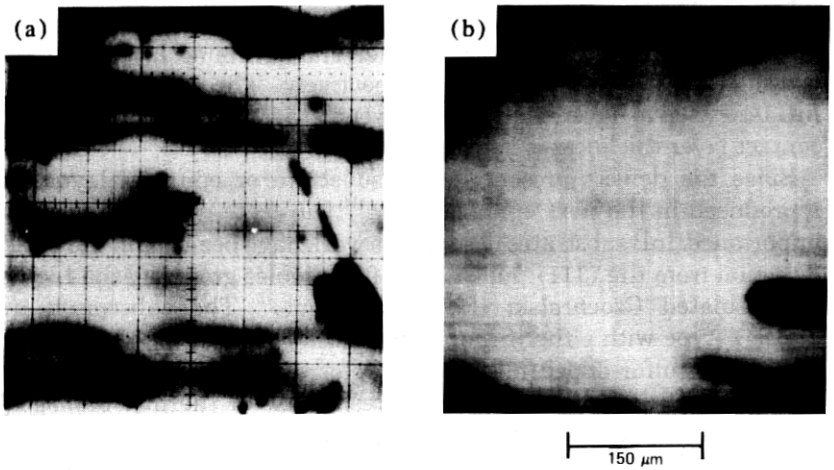

Fig. 2—Spatially resolved photoluminescence map of: (a) InP substrate subjected to a high temperature treatment, and (b) InP buffer layer grown on a well-protected substrate.

previously protected substrate, as shown by the uniform and bright PL scan of the InP buffer layer in Fig. 2b.

The second to grow is the the active layer of $In_{0.7}Ga_{0.3}As_{0.64}P_{0.36}$, a composition corresponding to the 1.3-μm emission wavelength. Particular attention is paid to the reproducible growth of layers with that composition, precisely lattice-matched to the InP substrate. In particular, a close lattice match, $\Delta a/a$ smaller than 6×10^{-4}, is required to prevent formation of misfit dislocations.[24] These act as nonradiative recombination centers and thus reduce luminescence efficiency. A transmission cathodoluminescence (TCL) image of misfit dislocations forming a characteristic criss-cross pattern on [100] oriented layer is shown in Fig. 3. This InGaAsP layer had a lattice mismatch of 1×10^{-3}.

In our experience, epitaxial layer morphology is not affected by lattice mismatch; layers of 1.3-μm InGaAsP with $\Delta a/a \approx 2.4 \times 10^{-3}$ have been grown with excellent morphology. Thus, it is necessary to monitor lattice match with X-ray diffractometry. The lattice constant can be well-controlled by precise weighing of the Ga and As components (up to ± 25 μgrams in a 10-gm melt) and careful reproduction of the growth temperature. Phosphorus loss in the equilibration cycle is compensated by the presence of excess InP. Accurate temperature control during the active layer growth results in reduced compositional

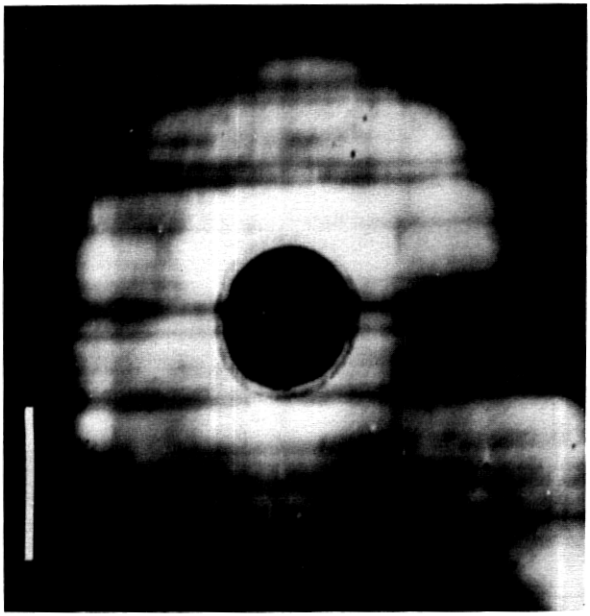

Fig. 3—Transmission cathodoluminescence (TCL) image of ⟨100⟩ misfit dislocations in a wafer with $\Delta a/a = 0.10$ percent.

grading. Compositional grading is especially pronounced for alloy compositions close to 1.3 μm.[25] The degree of compositional uniformity, obtained on a fairly routine basis, is demonstrated in a double X-ray spectrometer scan shown in Fig. 4. Double X-ray technique is used to fully resolve X-ray reflection width. The stronger peak originates in the InP buffer layer and the substrate, a much weaker and broader one, is due to the quaternary layer. The width of the InGaAsP reflection in this layer, ~60s of arc, is attributed to compositional grading in the direction of growth, i.e., along the thickness of the epitaxial layer. Larger grading results in broadening of the LED emission line width. In comparison, the width of the InP reflection is ~10s of arc, indicating the absence of any broadening because of thermal damage in the substrate.

The most common defects present in the epitaxial layers of InP and InGaAsP are inclusions of In. These originate at either meltback or wipe-off stages of the growth cycle and greatly reduce device yield and

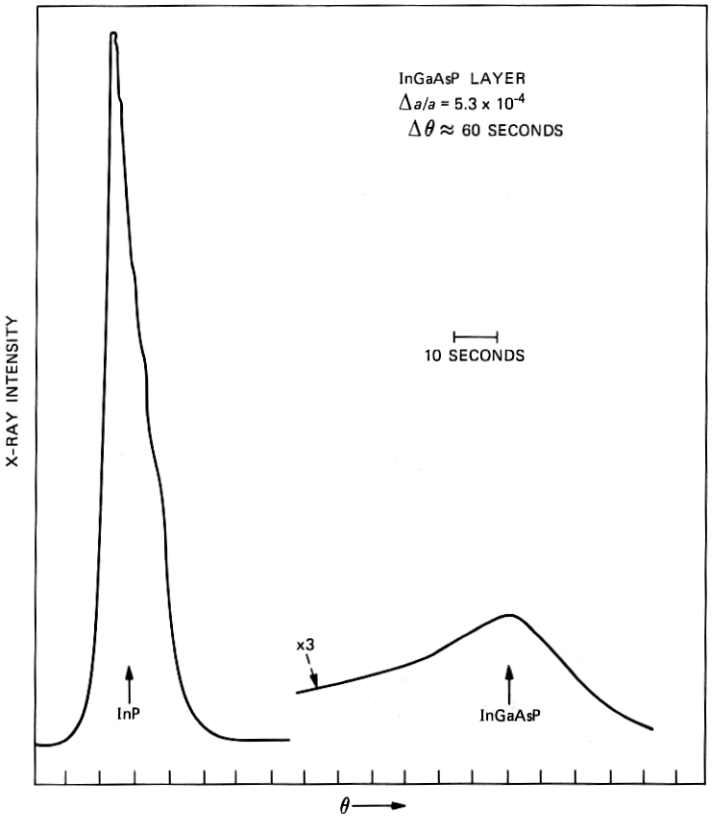

Fig. 4—Double X-ray diffraction scan of a device wafer. The width of the InGaAsP peak reveals a low degree of compositional grading.

reliability. A dramatic example of the wipe-off-related problem is shown in Fig. 5a. The InGaAsP active layer imaged in this Nomarski micrograph has been grown on a buffer layer that was not completely wiped off. The In inclusions left at the buffer surface locally prevent InGaAsP growth and produce holes in the active layer. This problem can be controlled by careful graphite boat design and maintenance of stringent wipe-off tolerances. Similarly, it is important to avoid melt contamination with particulate matter, such as carbon particles generated during prolonged equilibration baking. Figure 5b shows a more typical Nomarski image of the active layer. No defects were present throughout the entire 2.7-cm^2 wafer, resulting in excellent LED performance and uniformity. The horizontal lines visible in this image are growth lamellae characteristic of LPE-grown layers.

The most often used *p*-type dopant for the InP and InGaAsP layers is Zn. This dopant suffers from two well-known problems: high distribution coefficient and very high vapor pressure.[26] These can result in the contamination of the neighboring melts with concomitant junction misplacement into the buffer layer. This type of contamination is readily controlled by covering the melt wells and reducing the amount of Zn added. The undoped active layer is in fact grown as *n*-type material, and formation of the *p-n* junction is obtained by diffusion of Zn from the *p*-InP confining layer, as shown schematically in Fig. 6. To keep the *p-n* junction within the active layer, the amount of Zn in the InP confining layer must be kept low. However, to assure adequate electrical contact to the *p*-InP layer its doping level must be as high as

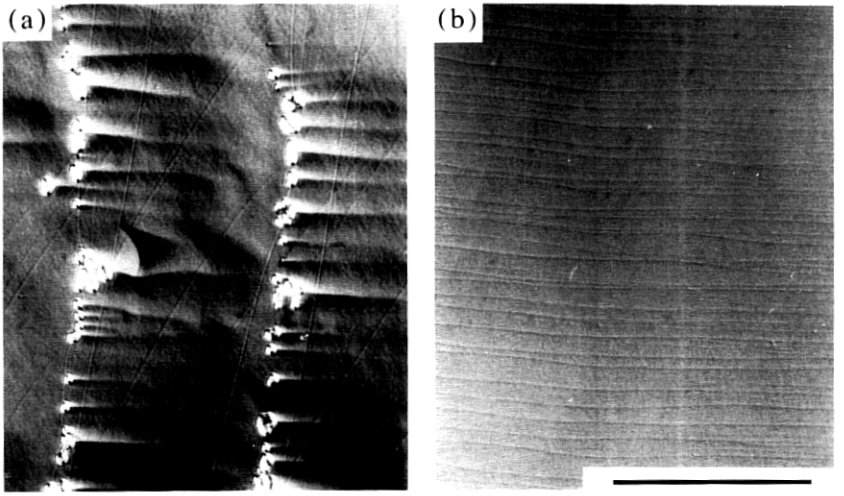

Fig. 5—A Nomarski micrograph (black bar = 100 μm) of the exposed InGaAsP active layer showing: (a) In inclusions owing to an incomplete wipe-off, and (b) inclusion-free surface of properly wiped-off layer.

possible. These conflicting requirements can be reconciled by reducing the doping level in the confining layer to 5×10^{17} cm^{-3} and adding a highly doped, $p \sim 2 \times 10^{19}$ cm^{-3}, InGaAsP contact layer. Thus, diffusion out of the contact and confining layers is used to form the p-n junction, the position of which can be well-controlled within the active layer. The influence of the junction position on LED performance is discussed in Section IV. In addition, contact resistance to the InGaAsP layer is found to be lower than that possible to the InP layer, as discussed in the LED fabrication section.

III. DEVICE FABRICATION

To obtain high-power, reliable LEDs, a great deal of attention must be devoted to processing procedures. A sequence of processing steps developed for the large-scale manufacture of the 1.3-μm InGaAsP LED is described in this section, with particular attention given to stress reduction and yield improvement. A typical processing flow chart is shown in Fig. 7. Device fabrication starts with the thinning of the LPE wafer from ~400 to approximately 100 μm. This is done by chemical-mechanical polishing with a bromine-methanol solution of less than 1

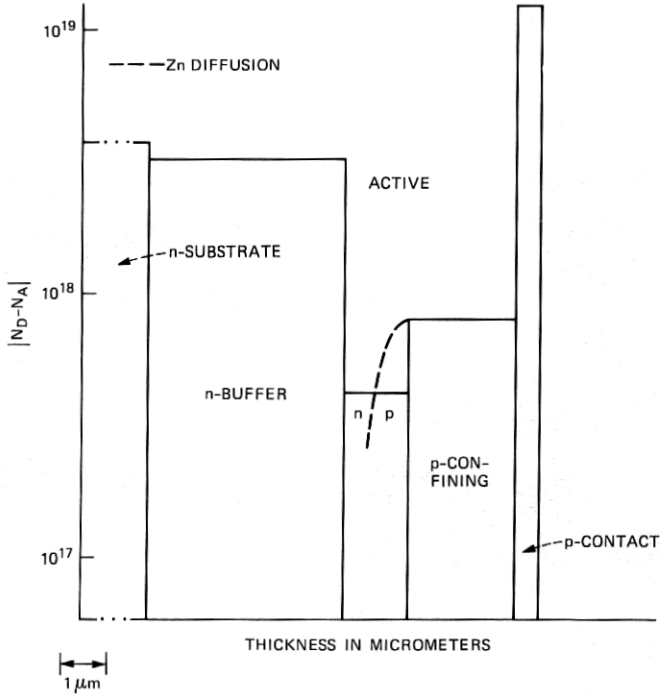

Fig. 6—A schematic diagram of the wafer structure indicating doping types and the Zn diffusion front.

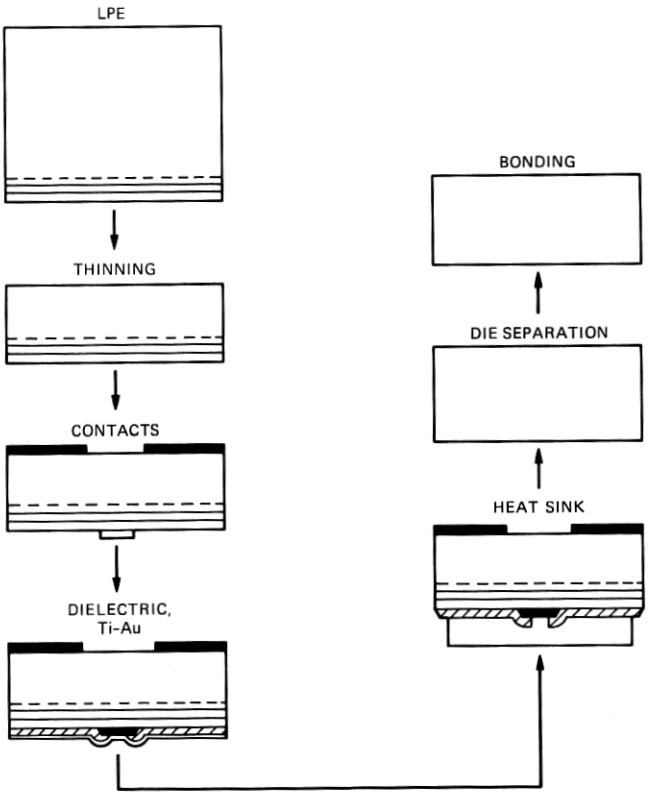

Fig. 7—Schematic processing diagram for a dielectric-isolated LED.

percent. Preliminary mechanical grinding is avoided to prevent formation of deep scratches and to minimize stresses. The finished substrate side should be mirror-like and free of polishing scratches since these affect light emission. After thinning, contacts on both sides are evaporated through a matched pair of shadow masks. Prior to contact deposition, careful cleaning with standard solvents followed by a 1-minute etch in 1:1 HF/H_2O solution are performed. The last etch is important for removal of surface oxides to ensure contact adherence and reproducibility of contact resistance. All the contacts are deposited by *e*-gun evaporation in vacuum of better than 10^{-6} torr. The *p*-contact metallization consists of an 800Å-thick layer of 1 wt-percent Be in Au alloy, deposited from an alloy source of the same composition, followed by a 2100Å-thick layer of Au. The BeAu alloy is prepared in advance and maintains its composition owing to nearly congruent evaporation of these two metals. The *n*-contact consists of a "sandwich" of 2000Å of Au, 500Å of Sn, and another overlay of gold at least 10 kÅ thick. The metallizations are alloyed in a N_2-H_2 flow and a fixed alloying time

of 8 minutes at 420°C is used. The order of metal layers in the *n*-contact is essential for low contact resistance and good bondability. When the first layer of Au is omitted and Sn is deposited directly on the semiconductor, contact morphology and adherence degrade owing to the well-known Sn-Au interdiffusion.[27] In contrast, the layered metallization results in a smooth contact of excellent uniformity and bondability.

Following ohmic contact deposition a dielectric film is placed on the *p*-surface. This film of plasma-deposited SiO_2 is used to electrically isolate the exposed surface of the *p*-layer and restrict the current flow to the *p*-contact area. The SiO_2 film should be sufficiently thick to prevent pinhole formation and yet as thin as possible to minimize the stress on the semiconductor. A dramatic example of dielectric stress-induced ⟨110⟩ dark-line defects in the *p*-InP confining layer is shown in a TCL image of Fig. 8. While these DLDs do not propagate into the active layer, LEDs in which they have been induced degrade extremely fast. This problem does not arise when the SiO_2 layer thickness is reduced to ~1000Å and the deposition conditions are adjusted to minimize stress. Next, the SiO_2 layer above the contact is photolithographically removed from an area about half the diameter of the contact. For instance, for the 25-μm diameter *p*-contact, a dielectric opening of ~12 μm is used. The small opening results in the metal contact cushioning the stress of the dielectric edge. The SiO_2 and the photoresist are stripped from this area in an O_2 plasma. It is important to assure cleanliness of the dielectric openings to obtain stable, low-forward-voltage devices.

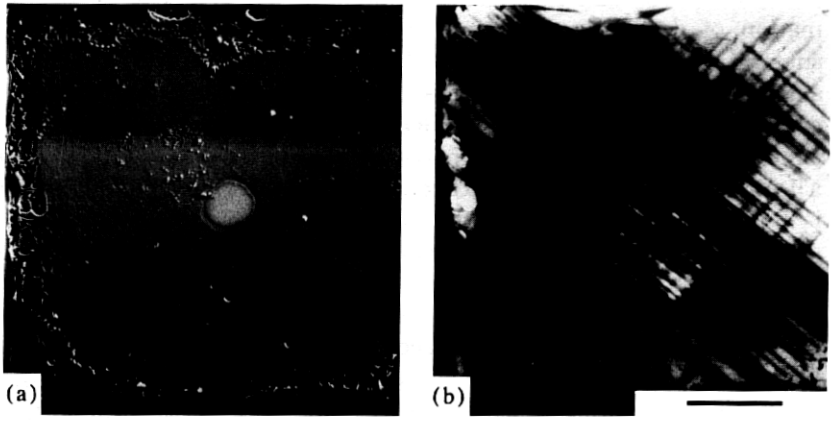

Fig. 8—Dark line defects induced by the dielectric stress in the *p*-InP confining layer: (a) Secondary electron image of the *p*-side of a rapidly degraded LED. The contact area is visible in the center. (b) TCL image showing ⟨110⟩ DLDs throughout the entire device.

A layer of Ti (1000Å) and a Au overlay (3000Å) are subsequently deposited over the full surface of the *p*-side, again by *e*-gun evaporation, and a 20-μm thick Au heatsink is electroplated. A Ti layer is used for good adhesion between SiO_2 and the heatsink. The heatsinks are formed in a photolithographically defined 20-mil-square pad pattern centered around the *p*-contact. The discontinuous Au film reduces wafer stress and makes diamond saw dicing easier. The "streets" in the heatsink pattern, similar to the *n*-type metallization squares, are aligned in the ⟨100⟩ direction. Misalignment tends to cause cleaving along ⟨110⟩ direction during the dicing operation and results in chip breakage. The dicing damage is removed by a ~30s etch in Br-methanol solution, which completes the processing sequence.

A recently described simplified processing sequence in which the dielectric layer and the subsequent photolithography are eliminated is also being used.[29] In this process, schematically shown in Fig. 9, current confinement is achieved through the formation of a Schottky barrier. The ohmic contacts are deposited and alloyed in the usual manner. Afterwards the entire *p*-surface, including the *p*-contact, is covered with a metal layer forming a highly resistive or non-ohmic contact (Schottky barrier) to the exposed semiconductor. This metal layer consists of 1000Å of Ti and 3000Å of Au. The initial layer of Ti adheres well to the semiconductor and forms the Schottky barrier. The processing sequence is again completed by electroplating heatsinks and dicing.

It is well known that the LED-fiber coupling efficiency improves as

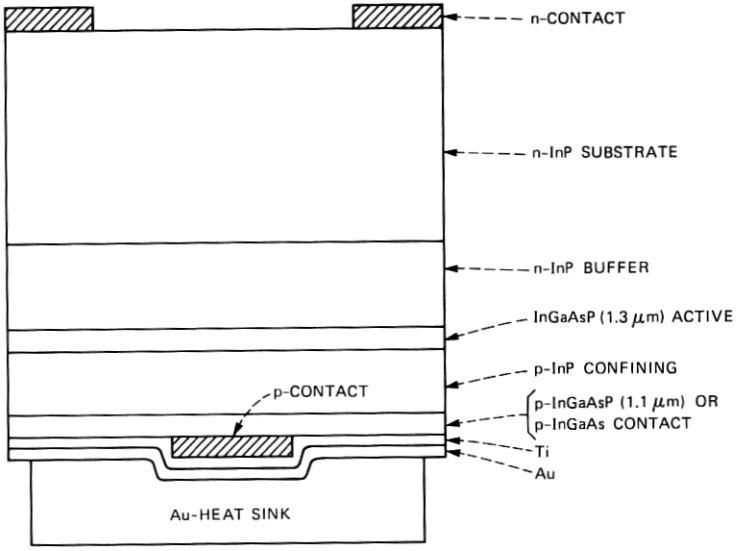

Fig. 9—Schematic structure of a Schottky-barrier isolated LED.

the light spot is made smaller than the fiber diameter. Similarly, the launched power can be increased by increasing the drive current. The resulting high-current density imposes stringent limits on the resistivity of the p-metallization. The resistance of the p-contact is strongly dependent on the material doping level and composition of the contact layer. In particular, contact resistance to both InP and InGaAsP layers decreases rapidly with increased doping level.[29] However, the low saturation limit for Zn incorporation in epitaxial InP ($\sim 4 \times 10^{18}$ cm^{-3}) limits the specific contact resistance to $r_c \sim 7.5 \times 10^{-5} \Omega$ cm^2 (see Ref. 30). This value of the specific contact resistance is sufficiently low only for p-contacts $\gtrsim 50$ μm in diameter. Furthermore, an unusual metallurgical reaction between Au and InP results in a spreading and enlargement of the p-contact upon metallization alloying, making formation of very small contacts difficult.[29] In contrast, the solubility of Zn in InGaAsP layers saturates at a doping level of $\sim 2 \times 10^{19}$ cm^{-3}, resulting in a specific contact resistance of $r_c \sim 2 \times 10^{-5} \Omega$ for the alloy composition corresponding to the 1.2-μm bandgap.

This composition of the contact layer is typically chosen to avoid absorption of the 1.3-μm light and allow back-reflection from the p-contact. However, the contact resistance continues to decrease as the composition of the InGaAsP layer is changed toward the ternary (1.65-μm) InGaAs alloy.[31] The results of specific contact resistance measurements as a function of alloy composition are shown in Fig. 10. The lowest $r_c \sim 7 \times 10^{-6} \Omega$ cm^2 was obtained on the InGaAs layer. This value is about a factor of two lower than the r_c measured for the commonly used 1.2-μm InGaAsP and results in 25-μm-diameter p-

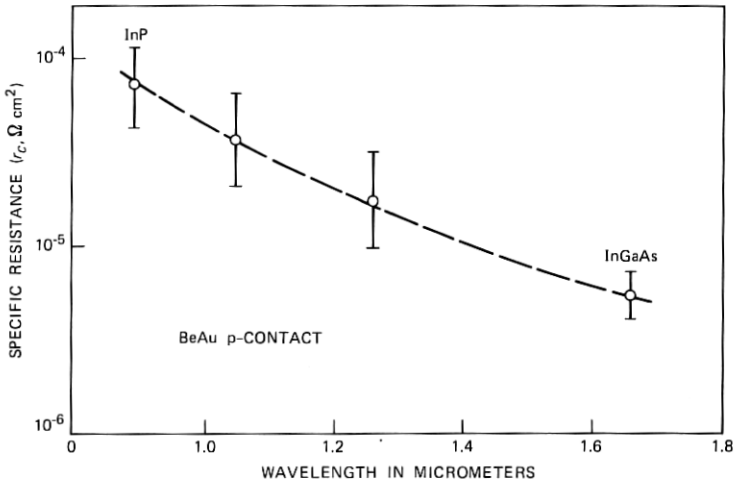

Fig. 10—Specific contact resistance as a function of alloy composition, from p-InP to p-InGaAs.

contact LEDs with a series resistance of less than 2Ω. LEDs incorporating such a ternary contact layer offer stable operation at very high current density without any appreciable reduction in the launched power, indicating that back-reflected light is not collected by the small acceptance angle of the fiber.

IV. LED PERFORMANCE

A number of parameters should be considered in determining LED performance in a transmission application. For data rates below ~100 Mb/s, increasing launched power increases repeater distance (at higher data rates modal dispersion begins to be important). The launched power decreases with increasing temperature and this temperature dependence also affects the repeater spacing. The injection level, on which the optical power depends, and the operating temperature may strongly influence reliability considerations, as discussed in the next paragraph. Finally, modulation bandwidth of the device which determines the maximum data rate, and the optical power are related and can be traded for each other by proper adjustments of the doping density and active layer thickness.

The light emitted into the air is plotted as a function of bias current in Fig. 11a at the three ambient temperatures of 0°, 25°, and 70°C. The *L-I* curves are clearly sublinear above 100 mA. At room temperature, a 50-percent increase in the forward current, up to 150 mA, increases the light output by ~20 percent or 1 dB. It should be remembered, however, that for 1.3-μm operation a 1-dB improvement in power output could correspond to a ~1-km increase in repeater distance. Such high current densities, up to 30 kA/cm^2 at 150 mA bias for a 25-μm-diameter *p*-contact device, are possible only for devices with a very low series resistance, $r_s \lesssim 3\Omega$, as discussed in the preceding section. At 25°C nearly 3 mW of optical power are emitted by these high-radiance devices. A higher power output into the air can be obtained for LEDs with larger *p*-contact areas, where the ohmic heating is reduced. However, small light-emitting areas are necessary for the efficient coupling of light into optical fibers.

The temperature dependence of the light output between −40°C and +70°C is plotted in more detail in Fig. 11b. The light-output/temperature characteristic follows the empirical relationship $L = L_0 \exp(-T/T_1)$, where the characteristic temperature T_1 of our devices ranges between 180 and 220 degrees and is independent of current.[32] Similarly, the functional form of $L(I)$ is independent of temperature. Thus, a temperature rise of 50°C above room ambient results in a power output decline of approximately 1 dB. While this temperature sensitivity is somewhat greater than that of comparable GaAlAs LEDs,

where $T_1 \approx 300$–$350°C$ has been observed, it is sufficiently small for LED operation without need for cooling devices.

Powers launched into fibers, as a function of fiber numerical aperture (NA) and core radius, are shown in Fig. 12. Two standard fibers, 0.23-NA, 50-μm core and 0.29-NA, 62.5-μm core are indicated by arrows. Closed circles denote butt-coupled powers; open circles and triangles refer to power launched using a lensing scheme in which a small sphere of high-index glass (~110 μm in diameter, $n \approx 1.9$) is mounted on the cleaved fiber end. All the devices have a 25-μm p-contact, active layer

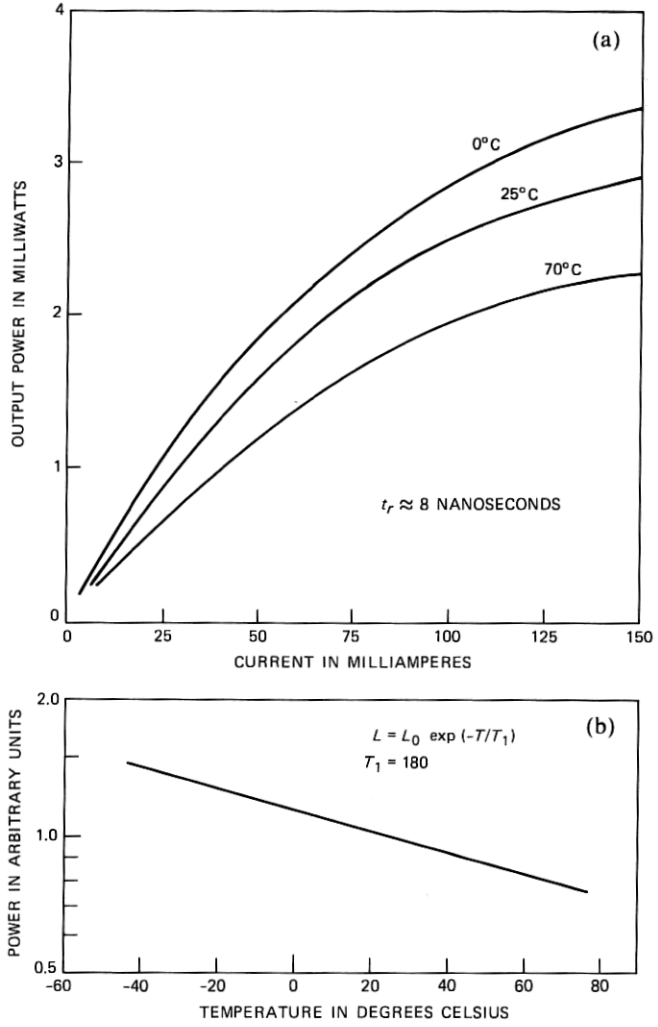

Fig. 11—(a) Light-current relation for a 25-μm diameter p-contact LED at three different ambient temperatures. (b) Temperature dependence of the light output at a constant current.

thickness of less than 0.7 μm, and a 10- to 90-percent risetimes of $\lesssim$4 ns. Because of current spreading the light spots are 30 to 35 μm in diameter, somewhat larger than the p-contact. No differences in current spreading or power launched have been found between dielectric and Schottky-isolated LEDs.

In the first approximation, the power coupled by an LED with a light-spot diameter d_s to a graded index fiber with a core d_f, when $d_s \leq d_f$, is given by

$$P = 1/2(\mathrm{NA})^2 P_0 \text{ butt coupled,} \qquad \text{and}$$

$$P = 1/2(\mathrm{NA})^2 M^2 P_0 \text{ lens coupled,}$$

where NA is the numerical aperture of the fiber, P_0 is the power radiated from the LED surface, and M is the magnification of the LED

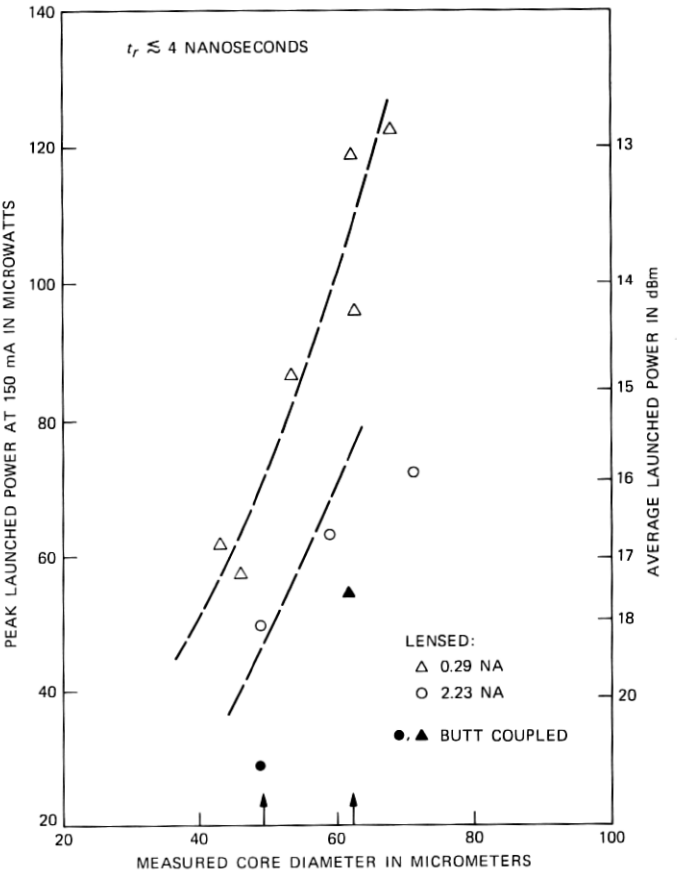

Fig. 12—Optical power launched into fiber as a function of NA and core radius. Two common fibers (0.23 NA, 50-μm core; 0.29 NA, 62.5-μm core) are indicated by arrows.

spot size by the lens. The latter has a maximum value when $M = d_f/d_s$, i.e., when the image just fills the fiber core. For a lensed system the coupled power, $P \approx (\mathrm{NA} \cdot d_f)^2$, as indicated by the dashed lines of Fig. 12. The data points and the dashed lines are in reasonably good agreement. The highest powers (peak) coupled by these fast LEDs were 50 and 120 μW into 50-μm and 62-μm core fibers, respectively. These powers are clearly a very strong function of the d_f/d_s ratio, the numerical aperture, and the lensing scheme used. Addition of an antireflection coating results in as much as a 20-percent increase in the power launched.[33] A coupling experiment with a 100-μm core 0.25-NA step index fiber achieved 410 μW of optical power. Such fibers, however, are not useful for optical communications.

The 1.3-μm LEDs discussed in Fig. 12 are very fast. Using a square-current pulse of 100 mA and a dc offset of 6 mA, risetimes of less than 4 ns are measured. The fall times are typically 1 to 2 ns longer. The fastest devices show risetimes close to 2 ns. As indicated by electron beam induced current (EBIC) scans, these thin active-layer (0.5 to 0.7 μm) devices have a p-n junction at the interface between the InGaAsP active layer and the n-InP buffer layer. The active layer is thus converted to p-type by Zn out diffusing from the confining p-InP layer. Hall measurements on InGaAsP layers grown under conditions simulating active-layer growth indicate doping level of $p \gtrsim 7 \times 10^{17}$ cm^{-3}. These LEDs have been successfully used in transmission experiments at 90-Mb/s rate.[34] On the basis of these risetime data, operation at 140 Mb/s is feasible without any speed-up circuitry.

The interplay of power and speed is well understood in GaAlAs LEDs.[35,36] The active layer of those devices can be doped directly with Ge and the resulting p-type doping level is well controlled. Thus, it is possible to change the doping level from $p \sim 1 \times 10^{17}$ cm^{-3} to $p \sim 1 \times 10^{19}$ cm^{-3} and the corresponding risetimes decrease from 25 to 4 ns. At the same time the power output is inversely proportional to the risetime, resulting in a constant power-bandwidth product in good agreement with theoretical models.[36] The results of a bandwidth-power study of 1.3-μm InGaAsP LEDs are summarized in Fig. 13. The 10- to 90-percent risetime (ns) is plotted on a log-log scale versus power launched into the larger fiber (62.5-μm core, 0.29 NA). Each data point represents an average of 10 devices from a single wafer. For the purpose of this study, the active-layer thickness is increased to 1.4 μm. It should be remembered that the p-n junction is formed by Zn diffusion from the confining layer and increased active-layer thickness permits better control of the diffusion front depth. The risetime correlates well with the amount of Zn added to the confining layer. The heavily Zn-doped devices have risetimes on the order of 4 to 6 ns, and the p-n junction is shifted all the way to the n-InP buffer interface.

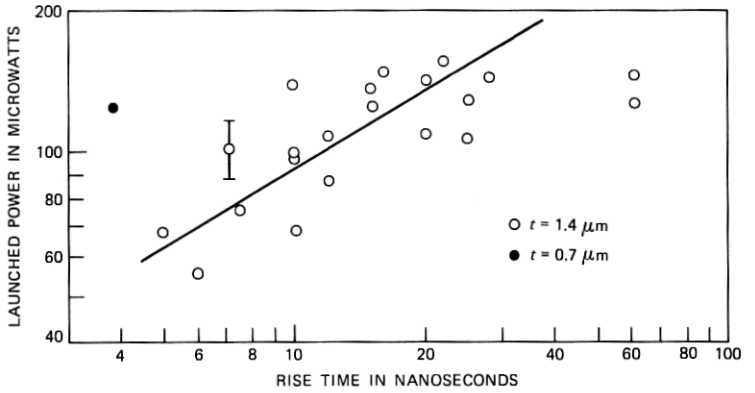

Fig. 13—Power versus risetime relationship for LEDs with a 1.4-μm thick active layer. Full dot demonstrates performance of 0.7-μm active-layer device.

As the amount of Zn is reduced, risetimes increase, up to 30 ns and output power increases by a factor of 2 to 3. However, in contrast to GaAlAs devices, the *p-n* junction displacement is gradually reduced, resulting in an *n*-type active layer. High powers of these LEDs demonstrate efficient hole injection into the InGaAsP layer. A simple model of a displaced junction gives a decay rate[37]

$$R = \frac{1}{\tau} = \omega \frac{1}{\tau_p} + (1 - \omega) \frac{1}{\tau_n},$$

where under high injection conditions

$$\omega = \left(1 + \frac{t_p}{t_n}\right)^{-1},$$

and $\tau_{n,p}$ refers to electron/hole lifetimes, respectively, t_p is the thickness of the active-layer region converted to *p*-type, and $t_n = t_{\text{active}} - t_p$. Thus, the decay rate is equal to the volume-weighted average of both minority carrier lifetimes. In our devices $\tau_n \approx 4$ ns and $\tau_p \geq 30$ ns. This finding is in good agreement with a previous observation[9] of increased power output for increased t_n/t_p. However, the *n*-active layer LEDs are slower and may not be useful for high-data-rate applications.

The best power result on thin (0.7 μm), active-layer LEDs is shown for comparison as a full circle in Fig. 13. The slower devices launch as much as 150 μW into 62-μm core fiber and up to 177 μW with an antireflection coating. The relatively high power and high speed of thin active-layer LEDs are interpreted in terms of higher injected carrier density and the resulting bimolecular recombination, which shortens the recombination lifetime.[38] It should, however, be noted that the 1.4-μm active-layer preparation is more reproducible and device results more uniform.

V. RELIABILITY

To estimate the reliability of LEDs for lightwave systems, life tests are performed under forward bias at elevated temperatures. The purpose is (*i*) to identify the failure modes relevant at operating temperatures, (*ii*) to find and eliminate the infant failure population, (*iii*) to determine the time, current, and temperature dependence of the degradation in light output to allow accurate extrapolations to end-of-life, and (*iv*) to determine the failure distribution so that failure rates can be calculated that reflect both the median life and the spread in the data. It is useful to begin by contrasting the failure modes in GaAlAs LEDs with what is known for quaternary LEDs.

The reliability of double heterostructure GaAs/GaAlAs has been studied extensively.[39,40] It is well known that ⟨100⟩ dark line defects (DLDs) form readily at grown-in dislocations in these devices. Their rate of growth is proportional to the square of current density (J^2), and independent of temperature. Depending upon the dislocation density in the epitaxial material, a certain fraction of devices (active area multiplied by the dislocation density) will fail catastrophically owing to DLD formation and must be screened out in a burn-in of about 100h. Under forward bias aging at 6 kA/cm^2 and T_J up to 250°C, the surviving devices remain free of DLDs but change gradually in light output owing to two competing processes with different time dependences and different activation energies.[40] These processes can be separated, and the degradation process is found to have an activation energy of 0.65 eV. This degradation is assumed to be due to the introduction of nonradiative defects at the junction. The projected mean-time-to-failure (MTTF) at 70°C is 4×10^6h. A notable feature of GaAlAs LED degradation is the small spread in times-to-failure for samples of diodes.[40] The failure distribution can be described as lognormal with $\sigma \cong 0.5$. This small σ coupled with the long MTTF gives very low estimated failure rates (e.g., a maximum of 10 FITs over a 20-year service life at $T_J = 70$°C).

In contrast, quaternary LEDs do not form ⟨100⟩ DLDs at threading dislocations, permitting much larger, ~10^4/cm^2, dislocation densities in InP substrates. Diodes with several dislocations in the active area have been aged at 10 kA/cm^2 for 2×10^4h without the appearance of DLDs.[41,42] The only dislocations that have been observed in electroluminescence after aging are ⟨110⟩ misfit lines in some diodes where the lattice mismatch between the buffer and quaternary layers is greater than 0.06 percent. In some cases the appearance of ⟨110⟩ lines accompanies a rapid drop in light output. The only infant failures observed in lattice-matched InGaAsP LEDs are due to instabilities in *I-Vs* or in light output. These instabilities result from shunt paths across the junction caused by In inclusions. A burn-in of 100h at 150

mA is done to screen out unstable devices. However, the burn-in yield for good, i.e., inclusion-free, wafers is almost 100 percent.

We report here the results of two series of accelerated aging experiments on dielectric isolated devices. In the first series, diodes labeled FC291 were fabricated from a wafer grown early in the quaternary LED development program. These were three-layer structures, i.e., without a contact layer, with 50-μm diameter contacts (the active-layer thickness was 0.7 μm). The epitaxial material contained a number of In inclusions up to ~10 μm in diameter, as discussed in Section II, and would be considered poor by present standards. The elapsed time for this series of experiments is now 1.5×10^4h. The second series of experiments is on wafer-labelled LP137, with an active-layer thickness of 1.4 μm. These are four-layer structures with 25-μm contacts, so that the current density J for a given device current is about four times that in FC291. These diodes were free of inclusions as shown by their electroluminescence patterns. The elapsed time for this series is 4×10^3h.

In FC291-type wafers, two modes of degradation have been identified: ⟨110⟩ DLD formation above 140°C and dark spot defect (DSD) formation at all temperatures. In the first mode, some diodes form ⟨110⟩ DLDs and drop rapidly in light output, even without bias. The DLDs originate at microscopic inclusion-like defects and are confined to the InP buffer layer. These ⟨110⟩ DLDs are similar to the dielectric stress-induced defects discussed in Section III. It is concluded that these DLDs are caused by thermal stress and that they grow by dislocation glide on the {111} slip planes. Because 140°C is apparently a threshold temperature for this effect, it will not be a relevant failure mode at operating temperatures.[43] This type of DLD has not been observed in recent wafers.

In analyzing the data for FC291, we eliminate all diodes that have ⟨110⟩ DLDs. In the remaining diodes, the light output falls linearly in time as shown in Fig. 14 and DSDs appear and grow. Because these LEDs do not fail abruptly, but rather drop gradually in light output, the definition of end-of-life should consider the overall system objective.[44] Since the repeater span is generally power-limited, it is desirable to allow as little power margin for end-of-life as possible, within system reliability requirements. For purposes of illustration, we define end-of-life as −1 dB change in output power. Figure 15 shows a typical failure distribution. It demonstrates that the failures are lognormally distributed with $\sigma = 0.6$. This σ is similar to that of GaAlAs devices and demonstrates excellent sample homogeneity. Figure 16 is an Arrhenius plot for median life under the various aging conditions. The activation energy is 0.85 eV. This activation energy is significantly larger than that obtained for the degradation of GaAlAs LEDs.

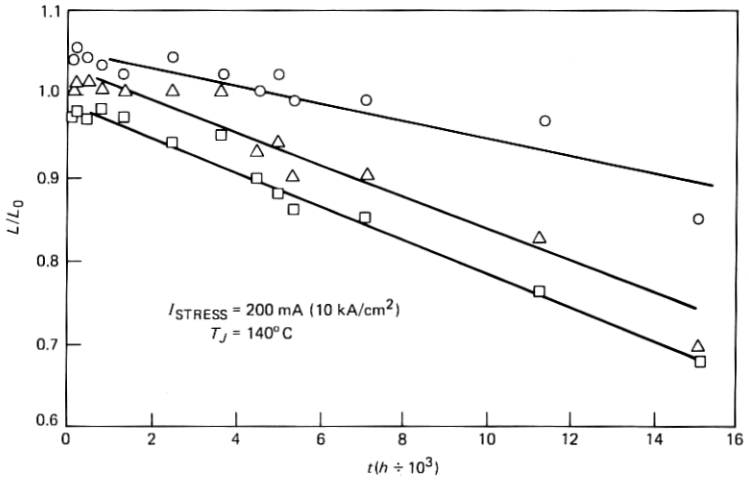

Fig. 14—Accelerated aging tests: light output versus time as a function of temperature for three typical diodes.

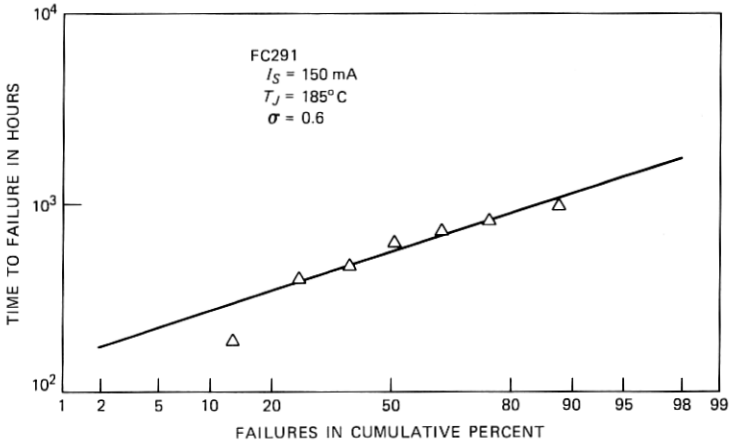

Fig. 15—Log-normal failure distribution typical of InGaAsP LED aging results.

Figure 16 also shows the results of experiments on wafer LP137. These diodes drop in light output linearly in time, but do *not* form DSDs. This is important, since DSD formation was believed to be a main degradation mechanism for InGaAsP LEDs. There is very little difference between median life (ML) for 20 kA/cm^2 and 40 kA/cm^2, suggesting that the failure mechanism (uniform degradation in light output) is not a strong function of current. Although the current density is four times higher in LP137 than in FC291, the ML has gone up by a factor of four. This probably reflects the improvement in the quality of the material.

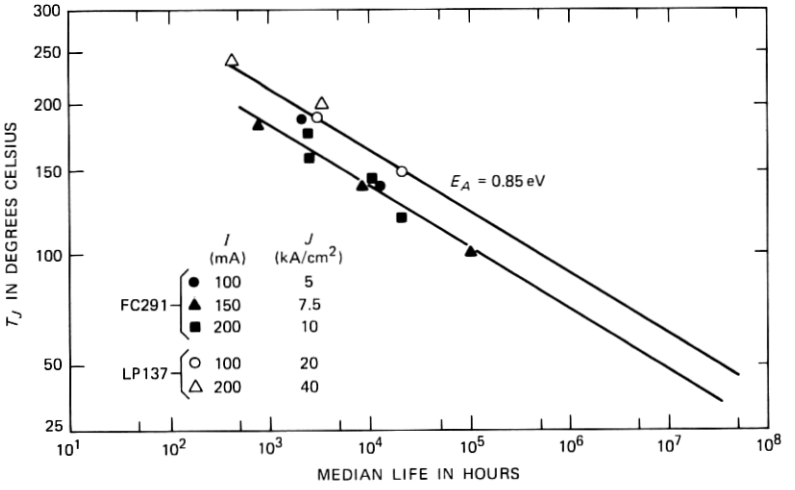

Fig. 16—Arrhenius plot of median life under various aging conditions. The activation energy is 0.85 eV.

The maximum operating temperature for these LEDs in most applications is 70°C. The 40 kA/cm^2 data projects median life of 4×10^6h at this temperature. For a service life of 20 years, using $\sigma = 0.6$, the projected failure rate is <1 FIT.[45] At 25°C median life of 3×10^8h is predicted. Higher reliability results if greater degradation is permitted. The system designer must trade off initial system performance for reliability objectives.

These reliability results are in good agreement with previous studies.[42,46] Thus, median life well in excess of 10^6 hours has been predicted at 25°C and current densities below 20 kA/cm^2. Similarly, the activation energy of 0.85 eV is consistent, within experimental uncertainties, with the 1.0 eV obtained previously. However, absence of DSDs in the high-quality wafer LP137 suggests that this degradation mechanism may be extrinsic. Further progress in material preparation and processing techniques should result in even better reliability of InGaAsP LEDs.

VI. SUMMARY

We have described the 1.3-μm InGaAsP LED developed for application in optical fiber transmission. This includes improvements and scale-up in the epitaxial growth procedures, careful design of the processing sequence, and optimization of the device structure. The resulting LED has a number of very attractive features. Its excellent optical powers allow repeater distances in the 10- to 20-km range for 62-μm fibers, depending on the cable loss. These long repeaterless spans can be realized at data rates of up to 90 Mb/s. This is accom-

plished with a relatively simple drive circuitry, as compared to lasers. In addition, the InGaAsP LED exhibits excellent thermal stability. As the ambient temperature is increased from 25°C to 70°C, the power output decreases by only ~1 dB. Finally, even at 70°C the median life exceeds 4×10^6h and the resulting failure rate is expected to be below 1 FIT.

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