

## CONTRIBUTORS TO THIS ISSUE

**Roy E. Anderson**, B.S.E.E., 1970, University of Illinois; M.S.E.E., 1972, University of Maryland; Bell Laboratories, 1970—. Mr. Anderson initially worked in the field of computer-controlled electrical measurement equipment for transmission facilities. His interest in computers led him into the area of designing real-time operating systems. Today, he is involved with developing a distributed digital electronic switch.

**Marshall E. Barton**, B.A., 1962, M.S. (Mathematics), 1964, Miami University; Bell Laboratories, 1964—. Mr. Barton initially was responsible for the development of support software for No. 2 ESS and No. 3 ESS. Since 1979 he has been associated with 3B20D DMERT, most recently as Supervisor of the Craft Interface Design Group.

**J. T. Beckett**, B.S. (Engineering), 1961, Harvey Mudd College; M.S.E.E., 1964, Ph.D. (Electrical Engineering), 1967, Case Western Reserve University; Bell Laboratories, 1967—. Part time lecturer, Electrical Engineering, Illinois Inst. of Tech., 1968–1975. Responsible for microcode on 3A processor and for the development of the 3B20D microcode and microcode tools. He also has been responsible for the development of software debugging tools. He is currently Supervisor of the No. 5 ESS Project Management Tool Development Group. Member, ACM, IEEE.

**Harry. L. Bosco**, B.S.E.E., 1972, Monmouth College, M.S.E.E., 1974, Polytechnic Institute of Brooklyn; Bell Laboratories, 1965—. Mr. Bosco has worked in data communications and hardware design for No. 4 ESS. He was promoted to Supervisor of the Network Design Group for No. 5 ESS in 1977 and to Head of the No. 5 ESS Line Interface and Peripheral Circuits Department in 1980. In 1981, he became Head of the No. 5 ESS Product Management Department, responsible for the generic planning, system architecture, and management of the No. 5 ESS product line. Member, Sigma Pi Sigma, Eta Kappa Nu.

**John M. Brown**, B.S.M.E., 1967, M.S. (M.E. & I.E.), 1969, University of Michigan; Bell Laboratories, 1969—. Mr. Brown started his career with Bell Laboratories by working on the development of 1A Technology apparatus. He has worked on the development of 1A Processor semiconductor stores and supervised the physical design of the 3B20D Processor. In 1980, he was appointed Head of a department responsible for the circuit design of the 3B20D Processor Control Frame and for physical design of the 3B Processor family.

**A. H. Budlong**, B.E.E., M.S. (Physics), Marquette University, 1950; Member of the teaching staff of the Department of Physics, Marquette University, 1948-1952; Bell Laboratories, 1953—. Since joining Bell Laboratories, Mr. Budlong has been engaged in exploratory development of electronic switching circuits and has conducted a group in charge of switching training at Bell Laboratories. He was involved in the development of the No. 1 electronic switching system in the areas of trunk and service circuits, and automatic message recording equipment, and in the design of high-speed communication buses and power facilities for the 1A Processor. He has been in charge of a group developing magnetic tape file systems, printers, and miscellaneous peripheral circuits for the 3B20D Processors. Mr. Budlong is the coauthor of a book entitled *Electronic Switching Theory and Circuits*. He is the Dean of the Undergraduate School and also a Professor of Electronic Engineering at the Midwest College of Engineering. Member, Sigma Pi Sigma and Pi Mu Epsilon.

**J. H. Campbell**, B.S. (Mathematics), 1964, Pittsburg State University; M.S., 1969, Ph.D, 1974 (Computer Science), Iowa State University; Bell Laboratories, 1974—. Since joining Bell Laboratories, Mr. Campbell has worked on the Extended Operating System (EOS) project and on the 3B20D/DMERT project doing operating systems development. Currently, he supervises a group engaged in the development and support of I/O drivers for real-time applications. Member, ACM, Sigma Xi.

**J. G. Chevalier**, B.E.E., 1951, Ohio State University; Bell Laboratories, 1956—. Mr. Chevalier has worked on a printed wiring board processes, applications for both military and telephone projects, connector design, studies of contact finishes, and the physical design and packaging of electronic equipment for switching systems. He presently supervises a group responsible for the development of packaging technologies for future versions of the 3B20D Processor.

**Noel X. DeLessio**, B.S.E.E., 1960, M.S.E.E., 1961, Ph.D. (Electrical Engineering), 1966, Polytechnic Institute of Brooklyn; Bell Laboratories, 1966—. Mr. DeLessio worked on SAFEGUARD system design and supervised guidance design for the SPRINT missile system. Subsequently, he supervised the Exploratory Development Group of the Operator System Laboratory and is currently Head of that Laboratory's Processor Applications Department.

**M. R. Dubman**, A.B., 1957, Princeton University; M.S., 1959, Massachusetts Institute of Technology; Ph.D., 1970, University of California-Los Angeles; Bell Laboratories, 1970—. From 1959 to 1970, Mr. Dubman was engaged in the development of statistical analysis techniques used in testing of Saturn/Apollo rocket engines for Rockwell International. At Bell Laboratories he has been involved in the development of software for the 1A and 3B20D Processors. Presently, he is Supervisor of a group responsible for the 3B20D system laboratories.

**Gary P. Eldredge**, B.S.E.E., 1971, M.S.E.E., 1971, Brigham Young University; Bell Laboratories, 1972—. Mr. Eldredge has designed a number of programs for the 1A Processor to assist debugging and updating software in operational field sites. Since 1977, he has been involved in the development, administration, and system testing of DMERT software. He recently was responsible for a group that designs utilities that are used in field sites to test, monitor, and maintain various parts of the software. He currently is Supervisor of the 3B20D fault recovery group. Member, Tau Beta Pi, Phi Kappa Phi, Sigma Xi.

**Robert L. Engram**, B.S.E.E., 1969, Howard University; M.S.E.E., 1973, Stanford University; Motorola, Portable Products Division, 1969-72; Bell Laboratories, 1972—. Prior to joining Bell Laboratories Mr. Engram was involved in design and development of analog and digital circuits for paging and terminal equipment. He received a patent for his work inhibiting shock falsing in a two-tone sequential decoder. Upon joining Bell Laboratories, Mr. Engram was initially involved in exploratory development of digital circuits and systems including AP3 and VSS. In 1977, he became Supervisor of Test Facilities for TSPS and later supervised a group performing Software Integration and Testing. He joined the 3B20D/DMERT Project in 1980 as Head of the Processor System Integrity Department and presently heads the Operating System Development Department. Member, IEEE, Tau Beta Pi, National Technical Association.

**Rudolph J. Frank**, B.S.E.E., 1966, Seattle University, M.S.E.E., 1968, Ph.D. (Electrical Engineering), 1971, Oregon State University; M.S. (Business Management), 1981, Stanford University; Pacific Northwest Bell, 1964-1966; Bell Laboratories, 1971—. At Pacific Northwest Bell, Mr. Frank was an electronics data processing supervisor in the comptroller's division. At Bell Laboratories he has worked on new feature planning and exploratory development in the Traffic Service Position System laboratory. In 1975, he was designated Bell

Laboratories Visiting Professor of Electrical Engineering at Southern University (Baton Rouge, La). Mr. Frank became Supervisor of the No. 4 ESS Network Management Control Group in 1976 and has managed several large software development projects. In 1980 he was awarded a Sloan fellowship in the School of Business at Stanford University. Mr. Frank is now Head of the Toll Digital Maintenance Planning and Development Department at Bell Laboratories, Member, IEEE, Eta Kappa Nu.

**Alan W. Fulton**, B.S.E.E., 1966, University of Arizona; M.S.E.E., 1967, Ph.D. (Electrical Engineering), 1971, Stanford University; Bell Laboratories, 1966—. Mr. Fulton has been involved in the design of processors for electronic switching systems. He currently is Head of the Processor Technology Department. This department is responsible for developing and integrating the silicon, packaging, and computer aided design tools required for processors. Member, Tau Beta Pi, Sigma Xi.

**Lee E. Gallaher**, B.S.E.E., 1951, M.S.E.E., 1956, Case Western Reserve University; Instructor in Electrical Engineering at Case Western Reserve University, 1952-1955; Bell Laboratories, 1955—. Mr. Gallaher has worked on memory systems for ESS including the Flying Spot Store, the Twister Memory and integrated circuit memories. He was promoted to Department Head in 1965 and was responsible for the design of the switch units for the No. 101 ESS and circuit designs for the No. 2 ESS and the No. 3 ESS. More recently he has been responsible for the architecture and development of the 3B20D processor. Member, IEEE, Tau Beta Pi, Sigma Xi, Eta Kappa Nu.

**Frank M. Goetz**, B.E.E., 1953, Manhattan College; M.S. (Mathematics), 1960, New York University; Bell Laboratories, 1953—. Mr. Goetz has worked on logic design, software development, and system design for electromechanical and electronic switching systems. He received five patents in the areas of electronic counters, error-correction circuitry, signal detection, and processor system design. Since 1962, he has been a Supervisor responsible for various aspects of electronic switching system and processor maintenance. At present, he is responsible for maintenance design of the 3B20S Processor. Member, IEEE, Eta Kappa Nu.

**Maureen Grzelakowski**, B.S., 1976, M.S., 1978 (Computer Science), Northwestern University; Bell Laboratories, 1977—. Ms. Grzelakowski was initially responsible for designing software development

environments for ESS projects. In 1980 she participated in the development of the DMERT nucleus. Since then she has supervised the Operating System Architecture and Planning, and Generic 2 Engineering Groups.

**Ronald E. Haglund**, B.S.E.E., 1960, M.S.E.E., 1963, and Ph.D. (Electrical Engineering), 1969, Iowa State University; Bell Laboratories, 1970—. Mr. Haglund initially worked on file store design for the No. 1A Processor. In 1979 Mr. Haglund became Supervisor of the 3B20D File Store Group with responsibility for the file stores for the 3B20D and other processors. He currently is Supervisor of the Peripheral Technology Group with responsibility for all 3B peripheral devices.

**Robert C. Hansen**, B.S.E.E., 1966, and M.S.E.E., 1969, Michigan State University; Ph.D. (Control Science), 1973, University of Minnesota; Bell Laboratories, 1973—. Mr. Hansen has worked on maintenance software for No. 4 ESS and the 3B20D. He is presently Supervisor of the Requirements and Architecture Group, concerned with feature evolution of the 3B20D. Member, IEEE, Tau Beta Pi.

**D. A. Harms**, B.S.E.E., 1963, M.S.E.E., 1965, University of Minnesota; Bell Laboratories, 1965—. Mr. Harms has been involved with the design of processors since 1967. Since 1970, he has supervised groups responsible for the design of memory subsystems, microstores, and peripherals for the No. 2 ESS, No. 2A ESS, No. 3 ESS, 3A Processor, and the 3B20D Processor. He is currently Supervisor of the Common Processor Circuits group responsible for the design of a diagnostic processor for 3B20S and for circuits incorporating the *Bellmac*<sup>TM</sup>-32A microprocessor in single board computers. Member, Eta Kappa Nu, Phi Theta Kappa.

**Irvine K. Hetherington**, B.S.E.E., 1966, Lehigh University; M.S.E.E., 1967, Stanford University; Bell Laboratories, 1972—. Mr. Hetherington initially was associated with exploratory development of integrated circuit analog switching networks for telecommunications applications. From 1972 to 1976, he was involved with the design of the microcontrol store and main memory system of the 3A Processor. Since 1977, Mr. Hetherington has had several design and supervisory responsibilities associated with the CPU and memory systems of the 3B20D Processor. He currently supervises the 3B20D Processor Data Communications Peripherals Group. Member, Tau Beta Pi, Eta Kappa Nu.

**J. Richard Kane**, B.S.E.E., 1968, University of Pittsburgh; M.S.E.E., 1970, Northwestern University; Ph.D. (Computer Science), 1973, Northwestern University; Bell Laboratories, 1968—. Mr. Kane initially worked in the areas of fault detection and system recovery for No. 4 ESS and later on testing tools. He system tested the first No. 4 ESS. Mr. Kane then supervised groups responsible for the development of the DMERT operating system, testing tools for the 3B20D Processor and developing local area networks. He currently supervises a group planning the design and development of new processors.

**W. F. Klinksiek**, B.S.M.E., 1966, M.S.M.E., 1967, and Ph.D. (Mechanical Engineering), 1971, Virginia Polytechnic Institute and State University; Bell Laboratories, 1971—. Mr. Klinksiek has worked on the physical design and packaging of the 1A Processor and the 3B20D Processor specializing in thermal and power engineering. He has supervised the development of packaging technology and computer automated design systems and managed software administration for the 3B20D. Recently, he was a Supervisor responsible for generic engineering, application interface, and application engineering for the 3B20D Processor System. Currently, he is Head of Processor Systems Customer Support Department. Member, Phi Kappa Phi, Tau Beta Pi, ASME.

**S. H. Kulpa**, B.S.M.E. 1972, Michigan Technological University; M.S.M.E., Stanford University; Bell Laboratories, 1973—. Mr. Kulpa has been involved with the design and development of the packaging technology for the 3B20D Processor. He currently is Supervisor of a physical design group.

**Peter Kusulas**, B.S.E.E., 1963, M.S.E.E., 1965, Rutgers University; Bell Laboratories 1963—. Mr. Kusulas has worked on the development of magnetic and semiconductor memory systems for the 101 ESS, No. 2 ESS, and the 3A and 3B20D Processors. Since 1980 he has supervised several groups engaged in the development of the *Bellmac*<sup>™</sup> microprocessor module and systems based upon it.

**N. A. Martellotto**, B.E.E., and B.S., Applied Mathematics, 1957, Georgia Institute of Technology; M.E.E., 1959, New York University; M.B.A., 1970, University of Chicago; Bell Laboratories, 1957—. Starting with the Bell System Data Processor project in 1957, where he did logic design and programming, Mr. Martellotto has been involved with computers and software development throughout his Bell Laboratories

career. Early projects include EPBX and No. 1 ESS. Mr. Martellotto holds a patent related to the basic notion of ESS generic programs. In 1966 he became Department Head of the Indian Hill Computation Center (IHCC). In 1976, he resumed design and development of ESS software development support programs and other related work. In late 1979, Mr. Martellotto became DMERT project manager and for the next two years was involved with all aspects of the project, from operating system development to field support. He is now Head of the Software Development Systems Department. Member, IEEE, Tau Beta Pi, Eta Kappa Nu.

**Peter S. McCabe**, B.S. (Engineering), 1956, Trinity College; B.S.E.E., 1957, Rensselaer Polytechnic Institute; Bell Laboratories, 1957—. Mr. McCabe has worked on memories for Nike-Zeus, digital circuits for the 101 EPBX, software design for the UNICOM, AUTO-VON, four-wire No. 1 ESS, and No. 4 ESS projects. Mr. McCabe supervised support software system development and program administration development and operation for No. 4 ESS. Since 1980 Mr. McCabe has supervised the performance measurements group for the DMERT project. Member, Tau Beta Pi, Eta Kappa Nu, Sigma Pi Sigma; associate member, Sigma Xi.

**JoAnne H. Miller**, B.S. (Mathematics), 1967, University of Michigan; M.S. (Computer Science), 1976, University of Colorado; GTE-Sylvania, 1968-1970; University of Colorado-Institute of Behavioral Science, 1971-1976; Bell Laboratories, 1976—. Prior to joining Bell Laboratories Ms. Miller was involved in system analysis and real-time programming for missile control and interactive computer graphic applications. Upon joining Bell Laboratories Ms. Miller was initially involved in No. 1 ESS software restructure design. Since early 1979 she has supervised groups responsible for the system testing and delivery of microprocessor software development systems, and design and development of several components of 3B20D/DMERT System, including the Recent Change/Verify System and equipment configuration data base. Currently, she supervises a group responsible for the field deployment and support of the 3B20D/DMERT system. Member, IEEE, ACM.

**H. L. Mitchell**, B.S.E.E., 1970, Rensselaer Polytechnic Institute; M.B.A., 1981, Illinois Benedictine College; Western Electric, 1970—. Mr. Mitchell's original assignment was to work with Bell Laboratories on system testing of the Safeguard MSR system. He has worked on

No. 4 ESS software development and testing and on 3B20D/DMERT system testing, system integration, and 3B20D Field Support. He is currently Department Chief, Call Processing and Residential Feature Development—1/1A ESS.

**Robert W. Mitze**, B.S. (Mathematics), 1969, California Institute of Technology; M.S. (Mathematics), M.S. (Computer Science), 1976, University of Wisconsin; Bell Laboratories, 1976—. Mr. Mitze has worked in the development of software engineering environments for the C language, project management of the DMERT operating system development, and distributed architecture specification for special-purpose applications. Since March 1981, he has been Head of the Advanced Operating System Development Department.

**B. G. Niedfeldt**, B.S.E.E., 1959, University of Maryland; M.S.E.E., 1961, New York University; Bell Laboratories, 1959–1962; Bellcomm, Inc., 1962–1970; Bell Laboratories, 1970—. Mr. Niedfeldt was engaged in exploratory development of high-speed data terminals. While at Bellcomm, he participated in the evaluation of the guidance and navigation aspects of the Apollo lunar landing missions. He then joined the Safeguard project, working in the multiprocessor operating system area. In 1974, he joined the No. 4 ESS team and, among other things, was responsible for the first generic (4E0) system test and release. In 1977, he joined the 3B20D/DMERT software development team, and is presently Supervisor of the Operating System, Software Integrity and Data Base Systems Group. Member, Tau Beta Pi, Eta Kappa Nu, Phi Kappa Phi, and Omicron Delta Kappa.

**Leland D. Peterson**, B.S.M.E., 1971, Illinois Institute of Technology; M.S.M.E., 1974, Northwestern University; Bell Laboratories, 1966—. Mr. Peterson has been involved with physical design of the 1A Processor, Voice Storage System (VSS), 1A Attached Processor System, and the 3B20D family of processors. He has participated in exploratory physical design and in the development of new hardware packaging technology. Currently he is Supervisor of the Large Processor Physical Design Group.

**Ralph W. Peterson**, B.S. (Physics), 1961, Wayne State University; M.S.E.E., 1963, New York University; Bell Laboratories, 1961—. Mr. Peterson has worked on software development on several electronic switching systems, including extensive work on software development tools. He presently is Supervisor of the Processor Microcode Group,



responsible for the development of microcode for 3B Processors. Member, ACM, Eta Kappa Nu, Tau Beta Pi.

**John L. Quinn**, B.S.E., 1959, Stevens Institute of Technology; M.S.E.E., 1961, New York University; Bell Laboratories, 1959—. Mr. Quinn worked on the design and system testing of the No. 1 ESS. He has been Supervisor of groups concerned with ESS system testing and development of maintenance software. For the 1A Processor project he was responsible for the processor diagnostics and for CPU logic/fault simulation. During the development of the 3B20D Processor he was responsible for the Processor Control Unit diagnostics and for the diagnostic control programs. Member, IEEE, Eta Kappa Nu.

**Michael W. Rolund**, B.S.E.E., 1961, Cooper Union; M.S.E.E., 1963, New York University; Bell Laboratories, 1961—. Mr. Rolund has been involved with the development of memory systems and processors including No. 1 ESS, the 1A Processor, and the 3B processor family. He currently is Head of the Processor Design Department responsible for the 3B20D and its evolution. Member, IEEE, Tau Beta Pi.

**Bruce R. Rowland**, B.S., 1973, Michigan State University; M.S., 1975, and Ph.D. (Computer Science), 1977, University of Wisconsin-Madison; Bell Laboratories, 1977—. Mr. Rowland began work in the area of languages and compilers, where he helped to extend the C programming language and coordinated the development of compilation tools for four processors, including the 3B20D Processor. He currently is supervising a group planning the development of 3B Processor networking and doing exploratory work in computer system design.

**Jack M. Scanlon**, B.S. (Applied Science), 1964, University of Toronto; M.S.E.E., 1965, Cornell University; Bell Laboratories 1965—. Mr. Scanlon joined Bell Laboratories in 1965, and initially worked on fault-diagnosis, resolution, and recovery techniques for the Bell System's No. 1 ESS. He also worked on a missile flight simulator for the Safeguard project. In 1968, he became Supervisor of the No. 1 ESS Call Program Group, responsible for the development of new customer call-features. In 1971, he joined the initial development team for No. 4 ESS with responsibility for system design and call-handling software. In 1974, he was promoted to Head of the No. 4 ESS System Design and Operations Department, where he was responsible for design of new capabilities for No. 4 ESS in domestic and international

applications, and for exploratory work on new software techniques. In 1977, he became Director of a Laboratory where he was responsible for the exploration of a secure voice/data communications system for the government. In June 1979, he was appointed Executive Director, Processor and Common Software Systems Division. In November 1982 he was appointed to the newly created position of Vice President, Processors, Western Electric. This work involves development of processors, microprocessors, *UNIX*\* operating systems, and programming languages and tools for Bell System applications. Mr. Scanlon has been granted four patents in processor design and electronic switching system design. He has published numerous articles on processor design for real-time, time-shared systems, electronic switching systems design, and software development techniques. Member, Computer Science Board of the National Academy of Sciences, IEEE.

**D. A. Schmitt**, B.S.E.E., 1965, St. Louis University; M.S. (Mathematics), 1968, Stevens Institute of Technology; Southwestern Bell, 1962-1965; Bell Laboratories, 1965-1969 and 1973—. At Bell Laboratories, Mr. Schmitt has been involved in the TSPS, No. 3 ESS, and VSS projects. He currently is in charge of the DMERT Operating System Architecture Department. Member, Eta Kappa Nu, Pi Mu Epsilon, Alpha Sigma Nu.

**W. C. Schwartz**, B.S.E.E., 1966, Purdue University; M.S.E.E., 1967, University of Michigan; Bell Laboratories, 1966—. Mr. Schwartz has worked on No. 4 ESS call-processing and fault-recovery software subsystems, software testing methodologies, and logic analysis and simulation systems. More recently, he was the generic engineer and application interface for DMERT. He currently is Supervisor of the Operating System Group in the Processor and Operating Systems Development Laboratory. Member, IEEE, Tau Beta Pi, Sigma Xi.

**Wing N. Toy**, B.S.E.E., 1950, and M.S.E.E., 1952, University of Illinois, and Ph.D. (Electrical Engineering), 1969, University of Pennsylvania; Bell Laboratories, 1952—. Mr. Toy has been involved in the design of highly reliable processors for the Bell System electronic switching systems and other telephone-related applications for the past 25 years. He was on the Faculty of the Computer Science Division of Electrical Engineering at the University of California, Berkeley, as a Visiting MacKay Lecturer during the 1973-1974 academic year. Mr.

---

\* Trademark of Bell Laboratories.

Toy holds 19 U.S. patents and is co-author of two books, *Mini/Microcomputer Hardware Design* and *Microprogrammed Control and Reliable Design of Small Computers*. He is currently Supervisor of the Voice/Data Technology Group. Fellow, IEEE.

**Susan S. Weber**, B.S. (Mathematics and Computer Science), 1977, Iowa State University; M.S. (Computer Science), 1978, Purdue University; Bell Laboratories, 1977—. Ms. Weber initially designed software development systems with her primary emphasis on source administration and object generation. Since becoming involved with DMERT, she has worked on both system update and field update and has participated in generic engineering and application interface issues. Currently, she is the Supervisor of the Field Update Group in the Operating System Development Department.

**R. J. Welsch**, B.S. (Mathematics), 1967, Marquette University; M.S. (Computer Science), 1972, Northwestern University; Bell Laboratories, 1967-1968; U.S. Army, 1968-1970; Bell Laboratories, 1970—. At Bell Laboratories, Mr. Welsch has had experience with No. 1 ESS/ADF, No. 4 ESS, and systems engineering for electromechanical switching systems. From 1974 to 1978, he was a member of the Program Administration and Support Program Group of the Operator Systems Laboratory (TSPS). From 1978 to 1980, Mr. Welsch was involved with developing software development systems utilizing PDP 11/70's running the *UNIX* operating system as front-end processors to larger IBM main frames. Since 1980, he has been involved with 3B20D/DMERT software development and administration. Mr. Welsch is currently Supervisor of the DMERT Administrative Software Systems Group.

**F. W. Wendland**, B.S.E.E., 1965, M.S.E.E., 1966, Cornell University; Bell Laboratories, 1966—. Mr. Wendland has been involved in the development of electromagnetic compatibility facilities and standards for ESS systems, automatic test facilities for ESS processor subsystems, 1A and 3B20D Processors, and I/O system architecture and design. He currently supervises a group working on the architecture and design of networking hardware for the 3B processor line. Member, IEEE.

**Neil O. Whittington**, B.S. (Physics), 1965, M.S. (Physics), 1970, Illinois State University; Bell Laboratories, 1970—. Mr. Whittington has worked on the development of software for the 1A Processor and the 3B20D Processor. He is presently Head of the Application Support Department, concerned with DMERT generic planning and application interfaces with the 3B20D. Member, IEEE.

**Robert M. Wolfe**, B.S.E.E., 1952, University of Louisville; M.S.E.E., 1957, Columbia University; Bell Laboratories, 1952—. From 1952 to 1962, Mr. Wolfe worked on applied research on ferromagnetic and ferroelectric devices and on data collection and data transmission systems. In 1962, he joined the Switching System Development area, where he headed the development of the Automatic Intercept System, the AMA Recording System, the Service Evaluation System, and the Network Control Point System. He is currently Head, Network Control Point Department. Member, ACM, IEEE.

**Robert H. Yacobellis**, B.S. (Mathematics), 1967, Carnegie-Mellon University; M.S., 1969, Ph.D., 1973 (Information Sciences), University of Chicago; Bell Laboratories, 1967—. Mr. Yacobellis worked initially on No. 1 ESS 4-wire AUTOVON (Government Switching). From 1969 through 1977 he was in No. 4 ESS working on overload control and later on program administration. In 1978 he became Supervisor of a group providing common loaders and simulators to ESS projects, and in 1980 became responsible for the 3B20D Field Update Group. He currently is in charge of documentation and software quality for the 3B20D. Member, Tau Beta Pi, ACM.