THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 62, No. 4, April 1983
Printed in U.S.A.

A Lithographic Mask System for MOS Fine-Line Process Development

By J. M. ANDREWS

(Manuscript received September 23, 1982)

A mask set, incorporating a group of seven test chips, has been designed for fine-line process development and process control. Although six lithographic levels are available, the masks are generally intended to be used only in subsets of two or three levels to minimize the delay encountered in obtaining electrical test results for whichever processes require investigation. The mask levels serve a variety of purposes for special process development experiments. Available structures include: metal-oxide-semiconductor capacitors, p-n junctions, guarded and unguarded Schottky barrier diodes, ohmic contacts, van der Pauw patterns, insulated gate field-effect transistors, gated diodes, resistors for sheet resistance and linewidth variations, and tapped electromigration test strings. It is not anticipated that a process engineer should ever need more than a maximum of four levels to achieve an appropriate experimental structure for process development. It is not the purpose of these masks to establish fine-line design rules. The masks are intended to be used primarily with standard photolithographic processing, and most device structures have been designed to tolerate up to 5 μm in misalignment errors. However, certain selected features have been coded in a diminishing sequence to a minimum of 1.0 μm for special fine-line investigations. A salient feature of this mask system is the option to interleave rapid turnaround photolithographic steps with fine-line X-ray patterning; therefore, some mask levels have been reissued for X-ray lithography.

I. INTRODUCTION

In the past, the development of new silicon integrated circuit processes was impeded by the fact that an adequate set of simple test structures usually could not be fabricated without resorting to the full set of six lithographic levels required by the Poon Tester Chips.[1] This set sometimes requires several months to fabricate if X-ray lithography is used. If device wafers could not be sacrificed, the processing engineer had to resort to simulating device structures, either by using metal dots of fixed areas on unpatterned oxides or deposited films, or by other schemes such as the use of offset circular windows using a pair of photolithographic steps.[2,3]

A set of photolithographic masks has been designed and is now available to fill the process development gap. The goal has been to provide the processing engineer with the means to simulate critical processing steps by introducing a monitor wafer, prepared in advance by one photolithographic step, and usually requiring only one more lithographic step of any type to obtain a structure ready for electrical testing.

The full set of fine-line process development masks consists of six photolithographic levels, but these have been designed to be utilized in subsets of 2, 3, or 4 levels only. Available structures include metal-oxide-semiconductor (MOS)* capacitors, contact windows, guarded and unguarded Schottky diodes, van der Pauw patterns, insulated gate field-effect transistors (IGFETs), gated diodes, and tapped electromigration test strings. Also available are large areas accessible for direct probing, for evaporation of MOS dots, or for Auger, scanning electron microscope (SEM), and transmission electron microscope (TEM) studies.

Section II contains a complete description of each of the devices that are available in the MOS mask set. The organization of the devices among each of seven test chips, the chip designations, the device assignments, wafer layout, design rules, and the alignment features are discussed in Section III. Section IV consists of a detailed description of each mask level separately, including the primary purpose for which the level is intended and the features available. Section IV also includes specific recommendations regarding which levels can be omitted with respect to the particular devices required or the experimental intent. Specific applications to silicon integrated circuit processing are discussed in Section V, and the MOS mask system is summarized in Section VI.

II. DEVICE DESCRIPTION

Most of the test structures in the lithographic mask system are MOS capacitors, because such two-terminal devices are easily fabricated. Normally, only two photolithographic operations are needed, and the first could usually be done on a large number of wafers before specific experiments are planned. Furthermore, the same patterns can be used

---

* Acronyms and abbreviations are defined fully in the Glossary at the end of this paper. Tables and figures are located at the end of the text.

to fabricate p-n junctions, Schottky diodes, or ohmic contacts to the substrate by simply omitting the gate oxidation. All such devices, with dimensions ranging from 1 to 500 μm, are contained on a single chip designated A. Larger devices, with dimensions ranging from 1000 to 4000 μm, are included on chips B and C1 through C4. The aim has been to provide maximum experimental flexibility by including a wide range of available device dimensions, which permits electrically active areas to span more than seven orders of magnitude. A summary of all devices contained in the MOS mask system is presented in Table I in the form of a device key, listing MOS device, nominal dimension, the chip assignment, and the appropriate probing pad number. Detailed descriptions of each device follow in Subsections 2.1 to 2.5. Dimensional data on all device structures are contained in the pad keys shown in Tables II through V.

2.1 Sixfold MOS capacitor group (HEXCAP)

The design of the lithographic mask system has evolved from a sixfold set of MOS capacitors (HEXCAP) that can be implemented at almost any stage of device processing to provide electrical characterization of dielectric layers.

2.1.1 FOXCAP and GOXCAP

The field oxide capacitor (FOXCAP) and gate oxide capacitor (GOXCAP) are shown in Fig. 1. For this pair of capacitors, the dimension L_1 increases through the sequence 50, 100, 200, 500, 1000, 2000, and 4000 μm. In all cases the dimension $L_2 = L_1 + 10$ μm, to conform with relaxed design rules to minimize registration errors (see Section 3.3). All FOXCAP and GOXCAP devices with $L_1 \leq 500$ μm are contained on the A chip, with peripheral probing pad locations coinciding with the Poon Tester[1] and the Process Monitor[4] chips. To facilitate MOS characterization of thick oxides or deposited dielectrics, a limited number of HEXCAP devices with L_1 equal to 1000 and 2000 μm were assigned to a larger chip B with area equal to that of ten standard Poon chips. The largest FOXCAP and GOXCAP devices on the C1 chips (see Section 3.1.3) are not square. Rectangular GOXCAP dimensions L_3 and L_4 for the largest devices have been selected so that

$$L_3L_4 = (4000\ \mu m)^2. \tag{1}$$

The rectangular structures of FOXCAP and GOXCAP are shown in Fig. 16. Specific values for L_3 and L_4 were selected so that the overall C1 chip dimensions could be adjusted to accommodate the contact metallization test chip (METEST) (see Sections 3.1.4 and 3.2).

In each HEXCAP group, the portions of the polysilicon (POLY) areas that overlay the gate and source and drain (GASAD) areas are equal. Thus, the capacitors formed over gate oxide (C_{GOX}) are equal among all elements of each HEXCAP group except FOXCAP. Furthermore, the total POLY areas are equal for FOXCAP, GOXCAP, and the devices with comb-shaped electrodes (POLYCOMB) to facilitate use with automatic testing programs. Thus, constant parasitic capacitance contributed by the field oxide (C_{FOX}) in parallel with C_{GOX} has been maintained among GOXCAP, GOXCOMB, and POLYCOMB (see following Section 2.1.2) for convenience in software development. Detailed dimensional data are contained in the pad keys, Tables II, III, and IV.

It should be clear from Fig. 1 that omission of the gate oxide in GOXCAP results in a structure suitable for ohmic contact, Schottky barrier diode, and p-n junction experiments. For this reason the dimension L_1 also decreases through the sequence 20, 15, 10, 7, 5, 4, 3, 2, 1.5, and 1.0 μm on the A chip. It is not expected, however, that the smallest GOXCAP windows would be routinely resolved by standard photolithographic processes. To resolve the smallest features, the GASAD mask level has been reissued for X-ray lithography. Because the X-ray target is nearly a point source, the finite separation between X-ray mask and the silicon substrate results in a slight magnification of the X-ray image. To compensate for the magnified X-ray image, a small demagnification of all features on the X-ray mask was required to make the X-ray lithographic level compatible with previous or subsequent optical lithographic levels. Alignment in the X-ray exposure facility, however, is done optically. Therefore the spacing between alignment features on the X-ray mask must remain the same as on the optical mask. With these modifications, X-ray lithography can be interleaved with more easily performed photolithographic steps.

The use of the GOXCAP structure to form a guarded Schottky diode is illustrated in Fig. 2, in which a guard ring with width W is diffused into the substrate before GASAD lithography. Guard-ring width options available in the mask set decrease through the sequence 10, 7, 5, 3, 2, and 0 μm (see Section 4.1). In all cases the guard ring has been centered on the GASAD boundary so that half its width extends into the contacting metal and reduces the effective contact area (see Fig. 2), so that:

$$A_{eff} = (L_1 - W)^2 \quad (\mu m^2). \tag{2}$$

For the cases in which $W \geq L_1$, the structure simply reduces to a p-n junction. Square or rectangular features have also been included in the GUARDRING level under the FOXCAP structures to provide the option of fabricating buried channel MOS capacitors[5–8] or to investigate the profiles of various ion implantations, such as those used to control threshold or punchthrough or for depletion loads.

2.1.2 GOXCOMB and POLYCOMB

To study peripheral effects or defects, structures with expanded gate-oxide/field-oxide periphery were included as the third HEXCAP element. This structure, abbreviated GOXCOMB, is shown in Fig. 3. On the A chip, the GOXCOMB structures comprise rectangular elements of width $d_1 = 25\ \mu m$, which are spaced $d_2 = 10\ \mu m$ apart. The total gate oxide areas of the two GOXCOMB structures on the A chip are $(200\ \mu m)^2$ and $(500\ \mu m)^2$. To further enhance peripheral effects, GOXCOMB structures have been included on the B and C2 chips with $d_1 = 5\ \mu m$ and $d_2 = 10\ \mu m$. Because of the decreased filling factor associated with reducing d_1 to 5 μm, it was not practical to keep the total gate oxide areas equal to the areas of the associated 1000-, 2000-, and 4000-μm GOXCAP structures; the actual areas are listed in Tables III and IV.

The POLYCOMB structure is similar to GOXCOMB except that the increased perimeter or peripheral expansion occurs at the gate-oxide/polysilicon boundary. The structural detail of POLYCOMB, the fourth HEXCAP element, is shown in Fig. 4. The chip assignments for POLYCOMB are the same as for GOXCOMB except for the 4000-μm structure, which is on the C3 chip. The same values for d_1 and d_2 apply to both COMB structures.

2.1.3 OVLAP and NOVLAP with FIELD PLATE

In some cases it is desirable to minimize parasitic capacitance in an MOS structure, i.e., the parallel capacitance composed of the area in which the gate electrode overlaps field oxide. The last pair of HEXCAP devices has been designed to minimize parasitic capacitance, consistent with the design rules discussed in Section 3.3. The OVLAP capacitor, shown on the left in Fig. 5, has a 5-μm overlap of the gate electrode onto the surrounding field oxide. The NOVLAP capacitor, shown on the right, has a gate electrode that has been retracted 5 μm from the GASAD boundary. The portion of the gate electrode that covers gate oxide in the OVLAP capacitor is equal to the area of the gate electrode in the NOVLAP capacitor. Both OVLAP and NOVLAP must be probed directly, because they are completely surrounded by a field plate that can be used to control the surface potential near the edges of each capacitor.

If a metallic silicide is formed in place of gate oxide, the resulting structure allows investigation of the effects of overlying metallization when excessive metallic penetration at contact window edges is suspected.[9] For these investigations it may be useful to include the GUARDRING option prior to silicide formation.

2.2 Sheet resistance group (SADSHEET and POLYSHEET)

Two three-terminal structures on the A chip can be used to obtain sheet resistance data from lines 400 μm long. Thus, accurate sheet resistance measurements can be made, even though the linewidths may deviate from the coded values because of unknown degrees of overetching or other process variations.

The left side of Fig. 6 shows the structure for measuring polysilicon sheet resistance (POLYSHEET). It consists of two 400-μm lines in series, but the coded linewidths are different: $W_1 = 5$ μm and $W_2 = 8$ μm. After processing, the actual linewidths may differ from the coded linewidths by a constant amount, ϵ. Assume that a positive value for ϵ corresponds to a linewidth loss from the coded value, W_i. If the resistance of each line is measured, it is possible to solve for both the sheet resistance and a constant linewidth loss, ϵ. It can be shown that

$$R_S = \frac{R_1 R_2}{R_1 - R_2} \cdot \frac{W_2 - W_1}{L} = 7.5\times10^{-3} \frac{R_1 R_2}{R_1 - R_2} \ (\Omega/\square) \tag{3}$$

and

$$\epsilon = \frac{R_1 W_1 - R_2 W_2}{R_1 - R_2} = \frac{5R_1 - 8R_2}{R_1 - R_2} \quad (\mu\text{m}). \tag{4}$$

A GUARDRING structure is included beneath some of the POLYSHEET lines. If the GUARDRING option were used, for example, to etch channels of various widths in a field oxide, the resulting POLYSHEET structure would provide information on poly-Si linewidths within oxide channels or straddling oxide steps.

Source-and-drain sheet resistance and linewidth variations can be determined from measurements on the structure shown on the right side of Fig. 6. The coded dimensions of the SADSHEET lines are exactly the same as for POLYSHEET, and eqs. (3) and (4) apply.

When the GUARDRING level precedes GASAD, some of the SADSHEET lines are imbedded into the guard-ring diffusion. Such a structure could be useful in determining the sheet resistance of a metallic silicide line for cases in which a low Schottky barrier height between the silicide and the substrate would interfere with electrical measurements.

2.3 van der Pauw group (VANDERPAUW)

The four-terminal symmetric structure shown in Fig. 7 has been provided on the A chip to make accurate determinations of polycrystalline silicon (poly-Si) sheet resistance in a way that is independent of the actual shape of the resistive pattern.[10] The poly-Si lines have been extended to the probing pads so that window and metallization lithography is not necessarily required. However, the option to have overlying metallization on the lines leading to the van der Pauw pattern, with windows to the underlying poly-Si, is available for unusual circumstances in which polysilicon sheet resistance may be very high.

The other VANDERPAUW structures are on the C4 chip, and consist of GUARDRING and GASAD patterns. The combinations POLY/GUARDRING and POLY/GASAD VANDERPAUW patterns are also included on the C4 chip to enable measurements of inversion layer sheet resistance[11] and to investigate CHANSTOP performance.

2.4 IGFET group

It is not anticipated that the IGFET group of devices will be utilized as often as the HEXCAP group of MOS capacitors, because the IGFETs require a minimum of four mask levels (GASAD, POLY, WINDOW, and METAL). For this reason, all IGFETs have been relegated to the B chip that has more available terminals than the A chip, although it may be less convenient for automatic probing.

Most of the IGFETs are included in one group with common sources and gates. The structure of the IGFET with $L = 20\ \mu m$ is shown in Fig. 8. All gates are 100 μm wide, and the gate lengths L descend through the sequence 20, 15, 10, 8, 6, 5, 4, 3, 2, 1.5, and 1.0 μm. It is not anticipated, however, that the shortest gates will be resolved with ordinary photolithographic processing. Therefore, the POLY mask level may also be reissued for X-ray lithography. Even with wide variations in processing, the range of gate lengths provides a means to determine the true (electrically active) channel length from a plot of β^{-1} versus the coded value for L, where β is the transconductance of the IGFET.

The GUARDRING option is available on all elements of the IGFET group. The guard ring straddles the GASAD feature on the three sides that are not adjacent to the gate, as shown in Fig. 9. Such a structure may be useful to minimize edge leakage when Schottky barrier sources and drains are investigated.

In some cases it is useful to make C-V (capacitance measured as a function of voltage) measurements of the gate electrode in an active IGFET. But practical IGFETs are generally designed to minimize gate capacitance in order to maximize switching speed, and the true gate capacitance is difficult to separate from parasitic capacitance. Therefore, four large-gate IGFETs have also been included on the B chip with gate dimensions descending through the sequence 500, 300, 200, and 100 μm square.

2.5 Gated diode group (GATODE)

The measurement of the depleted surface recombination velocity

s_0[12] is especially useful in evaluating the effectiveness of a low-temperature anneal to reduce surface state density[13] and to investigate the effects of radiation damage.[14,15] In the determination of s_0 it is necessary to directly control the surface potential near an MOS capacitor by means of a third electrode. This option has been made available by means of the gated diode group (GATODE), with dimensions decreasing through the sequence 500, 300, 200, and 100 μm square. The structure of the 100-μm gated diode is shown in Fig. 10. Obviously, a nearly equivalent structure could be realized by simply shorting the source to the drain of one of the large area IGFETs. The GATODE structures on the B chip differ from the IGFETs, however, in that the source-and-drain diffusions completely surround the gate electrode except for a 10-μm tab that connects the gate electrode to the probing pad. The GATODE structures are inverted from the usual gate-controlled diode in the sense that the p-n junction surrounds the gate electrode, whereas, the original gate-controlled diode structure consisted of an MOS capacitor in the form of a ring that surrounded a p-n junction.[16,17] The advantage of the GATODE structure is that better control of minority carrier production is possible when primary interest is centered on the properties of deeply depleted MOS capacitors.[18,19]

2.6 Contact metallization test chip (METEST)

Electromigration studies generally require high current densities, of the order of 10^6 A/cm^2, to achieve accelerated aging at a practical rate.[20] In the vicinity of contact windows, electromigration has been difficult or impossible to study, because the only test structure available has been the 100-window arrays on the Poon Tester A and C chips.[1] At the required current density, the sum of the voltage drops accumulated over a 100-window array often exceeds the breakdown voltage of the p-n junction that exists beneath each pair of windows. The contact metallization test chip D (METEST) has been designed to avoid large accumulated voltage drops by means of a tapped string of metal-to-diffusion windows, as shown in Fig. 11. Each tapped string is composed of series combinations of 1, 2, and 4 contact cells. Structural detail of one such contact cell is shown in Fig. 12 for a window size of 7 μm. With the D chip, a reliability engineer can select 2, 4, 6, 8, 10, or 14 windows in series, depending upon the particular breakdown characteristics of the structure. Each tapped string has been reproduced for a variety of contact window sizes, decreasing through the sequence 7, 5, 3, 2, 1.5, and 1.0 μm square. It is not expected, however, that the smallest windows would be routinely resolved by standard photolithographic processes. Therefore, the POLYCON mask level, which contains the contact windows for the METEST structures, has been reissued for X-ray lithography. The X-ray alignment features have been modified appropriately to make the X-ray lithographic level compatible with prior GASAD and subsequent POLY optical lithographic levels.

There has been a tendency to avoid rectangular contacts with large aspect ratios, i.e., $L/W > 3$. The reason is related to photolithographic exposure problems with very small contact windows, such as $W \leq 2$ μm. When additional contact area is required, parallel strings of square contact windows are often preferred to large, rectangular contacts. For this reason, the smallest contact windows on the D chip have been repeated in multiples of 4, 6, and 8 parallel windows for the 2-, 1.5-, and 1.0-μm windows, respectively. Structural detail of a multiple-window contact cell is shown in Fig. 13 for 4-window, 2-μm contacts. Obviously, the current does not divide evenly among the windows in such a multiple-window structure, but the extra contact windows can be regarded as providing an experimental backup when the first window fails. The multiple window strings also tend to increase continuity probability when working close to the limit of lithographic resolution.

III. ORGANIZATION

The lithographic mask system for fine-line process development has been organized on the wafer so that the simplest structures with the most convenient dimensions are available together on chip A. The included structures are HEXCAP, SADSHEET, POLYSHEET, and VANDERPAUW (see Section II). Perhaps the most unusual feature of the mask organization has stemmed from the enormous range of device sizes that have been made available to maximize experimental flexibility. Thus, structural dimensions ranging from 1 μm to 4000 μm are all present together on the same wafer. Furthermore, the largest areas can be used for direct probing, for evaporated MOS dots, or can be easily cleaved for Auger, SEM, TEM, X-ray, and other analytical investigations. It is the large range of device sizes (4-1/2 orders of magnitude) which has dictated chip designation and wafer layout.

3.1 Test chip designation

3.1.1 Chip A (1600 × 4096 μm)

Most of the devices with dimensions ranging between 1.0 and 500 μm are included on the A chip. A composite view of the POLY and WINDOW levels of the A chip is shown in Fig. 14. Both the dimensions of this chip and the placement of the 36 probing pads have been selected to coincide with the Poon Tester[1] and the Process Monitor[4] chips to facilitate automated probing with existing probe cards.

3.1.2 Chip B (8000 × 8192 μm)

The dimensions of the B chip are integral multiples (5 × 2) of the A chip to facilitate wafer layout (see Section 3.2), and the area is equal to that occupied by ten A chips. A composite view of the POLY, WINDOW, and METAL levels of the B chip is shown in Fig. 15. The size of the B chip has been selected to accommodate HEXCAP groups measuring 1000 and 2000 μm square, in the case of FOXCAP, GOXCAP, OVLAP, and NOVLAP. The GOXCOMB and POLYCOMB capacitors are nearly square, and have been laid out so that the equivalent areas are equal to the areas of the square capacitors (see Table III). Please note that to provide adequate resolution for illustration in Fig. 15, the width and spacing of the tines in POLYCOMB have been magnified 3X, and the number of tines has been accordingly reduced by a factor of 3 so that the overall dimensions remain unchanged. Accurate dimensional data on POLYCOMB can be measured from Fig. 15 by scaling down detail 3X. Areas and perimeters are listed in Table III. Also the gap between the field plate and the OVLAP and NOVLAP capacitors has been widened 3X. The IGFET arrays and gated diodes were assigned to the B chip for two reasons: (*i*) at least four photolithographic steps are required to realize completed devices, so it is anticipated that these will not be used as frequently as the two-level structures on the A chip; (*ii*) the IGFET and gated diode arrays require 23 additional probing pads that are not available on the A chip. To provide adequate resolution for illustration, the spacing between gates and sources and drains has been increased 3X in Fig. 15. In the gated diodes the space between gates and junctions has also been increased 3X.

3.1.3 Chip C (6400 × 8192 μm)

The largest MOS capacitors, with areas measuring (4000 μm)^2, had to be allocated to four separate chips. The C1 chip contains FOXCAP and GOXCAP capacitors with areas equal to (4000 μm)^2. A composite view of the POLY and WINDOW levels is shown in Fig. 16. The C2 chip contains a rectangular GOXCOMB structure with area somewhat reduced from the rectangular devices on chip C1; the exact coded areas are listed in Table IV. A composite view of the POLY and WINDOW levels is shown in Fig. 17. The C3 chip contains a rectangular POLYCOMB structure with area somewhat reduced from the rectangular devices on chip C1; the exact coded areas are listed in Table IV. A composite view of the POLY and WINDOW levels is shown in Fig. 18. To provide adequate resolution for illustration in Fig. 18, the width and spacing of the tines have been magnified 3X, and the number of tines has been accordingly reduced by a factor of 3 so that the overall dimensions remain unchanged. Accurate dimensional data can be measured from Fig. 18 by scaling down detail 3X. Areas and perimeters are listed in Table IV.

The C4 chip contains both OVLAP and NOVLAP rectangular capacitors with areas measuring $(4000\ \mu m)^2$ and surrounded by a field plate. A composite view of GUARDRING, GASAD, POLY, and WINDOW levels is shown in Fig. 19. For the purpose of illustration the gap between the field plate and the OVLAP and NOVLAP capacitors has been widened 3X in Fig. 19. All C chips measure $6400 \times 8192\ \mu m$. When combined with the D chip (see next section), the overall dimensions of the combination are exactly equal to the dimensions of the B chip or a 2×5 array of A chips.

3.1.4 Chip D (1600 × 4096 μm) METEST

A composite view of the POLY and WINDOW levels of the contact metallization test chip D (METEST) is shown in Fig. 20. Both the dimensions and the locations of the 36 probing pads of the METEST chip have been selected to coincide with the Poon Tester[1] and the Process Monitor[4] chips to facilitate automatic probing. It is expected that the tapped strings with 2-, 3-, 5-, and 7-μm windows will be used most extensively. These strings have been terminated on probing pad numbers 3, 4, 5, 6 (3 μm), 9, 10, 11, 12 (2 μm), 21, 22, 23, 24 (7 μm), and 27, 28, 29, 30 (5 μm) to coincide with existing metallization probing cards.

Detailed dimensional data for the D chip are listed in Table V. Table V differs from Tables II through IV in many respects, because the tapped strings were not intended to provide capacitance data. There are no GUARDRING features. Entries tabulated under GASAD tub refer to features straddling the indicated pad numbers, although all tubs within each string are connected in parallel after metallization with the POLY level. Entries tabulated under POLYCON window refer to the total cross-sectional area of a single tub input or output. However, current density is not expected to be uniform over any given window and especially among multiple windows. Entries tabulated under POLY are intended to aid in estimating string resistances from the sheet resistance of the metallization layer provided by the POLY pattern. Taps and ties are defined in Fig. 11, and the equivalent numbers of squares straddling each pair of pad numbers are indicated. The equivalent number of squares for the contact areas were not included, because these depend upon the sheet resistance of the underlying tubs.

3.2 Wafer layout

The location of each of the test chips described in the preceding section is shown in Fig. 21. The A chip is the most numerous, totaling 130 and arranged in blocks of 10 to form the cross-shaped pattern coded AX in Fig. 21. The number X, following A, denotes the width of the guard ring when the GUARDRING (N35) option is selected. The symbol A0 denotes unguarded devices. The arrangement of the A chips, which have been laid out to permit automatic probing with existing facilities, is obviously intended to reveal horizontal and vertical parametric trends on test wafers.

There are only twelve B chips, which contain 1000- and 2000-μm devices. When the GUARDRING (N35) option is selected, there are only two chips for each guard-ring width, i.e., 2, 3, 5, 7, and 10 μm. As in the case of the A chip, guard-ring width is represented by X in the notation BX, shown in Fig. 21. The asterisks denote undefined guard-ring diffusions or implantations that cover the entire chip for evaluation of guard-ring performance without a parallel Schottky diode.

There are six C1 and six C4 chips on the test wafer. In each case, three are unguarded and three have 10-μm guard rings, *viz.* C1-0 and C1-10 in Fig. 21. The C2 and C3 chips contain large GOXCOMB and POLYCOMB structures, respectively. Two are unguarded, *viz.* C2-0, and two have guard rings, *viz.* C2-10, in Fig. 21. In the case of GOXCOMB, the guard-ring width does not permit interdigitating the individual COMB elements, so the guard-ring option provides a buried diffused tub beneath the GASAD structure. As in the B chip, the asterisks denote undefined guard-ring diffusions or implantations.

The contact metallization test chip is denoted D in Fig. 21. There are a total of 40, which have been divided equally among the four quadrants of the wafer.

At the top and bottom and left and right are four alignment patterns that have been designed to permit aligning any mask to any other in any order (see Section 3.4). Also associated with each alignment pattern are two TEM test chips that have been specially designed to facilitate transmission electron microscopic (TEM) analysis.[21] (See Section 3.5.)

3.3 Design rules

The lithographic mask system has been designed specifically for fine-line process development and process control. Since the masks are generally to be used with standard photolithographic processing, it obviously would be inappropriate to interpret data in terms of fine-line design rules. Consequently, most device structures have been designed to tolerate up to 5 μm in misalignment errors. Figure 22 is an example of such relaxed design rules, showing the source-gate structure of a typical element from the IGFET group (see Section 2.4). The same structure also applies to the junction contacts of the gated diode group (GATODE) (see Section 2.5). In general, all contact windows have a minimum width of 5 μm, and all overlapping regions are a minimum of 5 μm.

A number of exceptions exist, however. Most prevalent are the GOXCAP group (see Section 2.1.1), which has been deliberately continued to a minimum size of 1.0 μm to enable special experiments with nonstandard photolithographic processes or X-ray lithography. A similar philosophy has been applied to the entire contact metallization test chip D (METEST), which has been fully described in Section 2.6.

3.4 Alignment features

It is hoped that maximum flexibility has been achieved by the use of a modified version of the standard Perkin-Elmer projection (PEP) alignment features. These modified PEP (MOPEP) features are shown in Figs. 23a through f and are presented in the anticipated "normal" order or suggested sequences, i.e. GUARDRING, GASAD, POLYCON, POLY, WINDOW, and METAL. The upper set of MOPEP features in each of Figs. 23a through f corresponds to the "normal" processing sequence. Unlike alignment procedures for virtually all device codes, each mask in this lithographic system must be aligned to the immediately preceding level, because levels prior to the one immediately preceding introduce overlapping patterns. But the unique feature of the MOPEP alignment features is that any number of levels can be skipped. For example, it has been anticipated that a popular sequence may be GASAD followed by POLY only. The alignment feature remaining on the test wafer after GASAD lithography is shown in Fig. 23b. Alignment of POLY to GASAD corresponds to a "normal" processing sequence, so the second MOPEP feature in the upper half of Fig. 23d would have to be aligned to the second (right-hand) MOPEP feature in the upper half of Fig. 23b. The left-hand MOPEP feature in Fig. 23b is simply ignored, because the GUARDRING level was omitted.

The lower set of MOPEP alignment features in Figs. 23a through f have been included to enable an "inverted" processing sequence. Such an "inverted" processing sequence might be required for some unique or novel structure that was not originally intended or anticipated. For example, POLY features can be defined on the surface of an unpatterned field oxide. After oxidation, or deposition of an intermediate dielectric layer, it might be necessary to define additional conductive features of either poly-Si or metal directly over the original poly-Si features. This capability is available by using a "GASAD" level with reverse tone (see Table VI), consisting of opaque features within a transparent background, to produce conductive patterns in polysilicon or metal. Alignment is carried out by inserting the central MOPEP feature in the lower half of Fig. 23b into the right-hand MOPEP feature on the lower half of Fig. 23d, which would be the pattern left on the test wafer after POLY lithography. (Tone reversal is not applied to MOPEP features.)

To be consistent with the relaxed 5-μm design rules discussed in the preceding section, the right-hand MOPEP feature in the upper halves of Figs. 23a through f are all 25 μm wide. All of the other MOPEP features in the upper halves of Fig. 23b through e and all MOPEP features in the upper half of Fig. 23f are 20 μm wide. A similar scheme that provides 2.5-μm frames for alignment in inverted order applies to the lower halves of Figs. 23a through f. The 2.5-μm alignment frame has resulted from a compromise that should offset the effects of photolithographic processing variations, but proper alignment does require some judgment on behalf of the alignment operator to optimize registration of sequential mask levels.

3.5 TEM test chip

Sample preparation techniques for transmission electron microscopy (TEM) usually produce sections sufficiently thin over a region that may vary between 40 and 100 μm. All morphological features essential for process evaluation can be translated into the area for TEM study by a special test pattern 1 mm wide and approximately 6.7 mm long, and with a structural period of 29.5 μm. The TEM test pattern is shown in Fig. 24, showing gate oxide within regions defined by GASAD, contact windows formed by POLYCON, layers of poly-Si defined by POLY, and subsequent P-glass and metallization levels. Thus all windows, steps, and other peripheral features normally encountered in fine-line process development are reproduced over 200 times within each TEM test chip. Two TEM test chips have been placed symmetrically with respect to each MOPEP alignment feature (see Fig. 21), and no active device areas have been sacrificed. A total of eight TEM test chips have been incorporated into the lithographic mask system, and the feature boundaries of each TEM test chip are oriented orthogonal to a ⟨100⟩ cleavage plane so that the cross section shown in Fig. 24 can be readily obtained from widely separated areas of the wafer. The TEM test chip shown in Fig. 24 differs from the one published by Sheng and Marcus,[21] partially because the chip in Fig. 24 was designed for a fine-line process that does not involve selective oxidation.

IV. MASK LEVELS

The six mask levels that comprise the normal tone portion of the lithographic mask system are listed in the upper part of Table VI and are intended to be used with positive photoresist. The suggested sequence reflects the primary purpose for which each level was intended; a few examples are shown in Table VII. Each mask level contains four full sets of MOPEP alignment features, corresponding to "normal" and "inverted" processing sequences. Thus, it is possible to align any mask level to any other, thereby permitting novel device structures with processing sequences that have not been anticipated. (See Section 3.4 for alignment details.) The three levels that have been issued in reverse tone are shown in the lower part of Table VI. They have been intended for use with negative photoresist, uniform gold metallization, selective oxidation or other special processes.

4.1 GUARDRING

The GUARDRING level would generally be omitted for most MOS processing investigations. In a sense, it may be viewed as being analogous to the isolation tub diffusion that occurs in CMOS processing prior to GASAD. The principal purpose of the guard ring is to provide p-n junctions that straddle the boundaries of Schottky barrier diodes to electrically isolate metallization edges that often obscure barrier characterization. The GUARDRING level is unusual because it comprises a subset of six patterns that provide guard-ring widths of 10, 7, 5, 3, 2, and 0 μm. The location of each of these subsets is indicated in Fig. 21 by the final hyphened integers X, i.e., C1-X. Each guard ring is located such that it frames each GASAD boundary symmetrically. In the case of the smallest GASAD features, the area enclosed by the larger GUARDRING features vanishes, and a p-n junction is formed, which is useful for evaluating guard-ring performance. The asterisks denote undefined diffused or implanted areas that cover the entire chip. These chips can also be used to characterize the guard rings independently from the other features or to evaluate ion implantation profiles (see Section 2.1.1).

4.2 GASAD

The GASAD level is normally the first level that would be used for MOS process development and monitoring. The principal purpose of the GASAD level is to open up areas in the field oxide in preparation for a possible ion implantation, for threshold control, followed by gate oxidation. If gate oxidation is omitted, however, the GASAD level provides a range of areas for investigations of contact resistance, Schottky barrier diodes, and p-n junctions. Most of the patterns provided by GASAD are square and progressively increase in size through the sequence 1.0, 1.5, 2, 3, 4, 5, 7, 10, 15, 20, 50, 100, 200, 500, 1000, 2000, and 4000 μm. At 200 μm and above, comb-like structures (GOXCOMB) are included in the GASAD level for investigation of peripheral effects and defects. The 200- and 500-μm GOXCOMB structures consist of a series of 25-μm slots separated by 10 μm of field oxide (see Fig. 3). All of the slots are interconnected to guarantee equalization of surface potential. The choice of the relatively large slots assures that all of the MOS capacitors within HEXCAP will have nearly equal gate areas despite typical variations in linewidth owing to processing variables. Obviously, GOXCOMB can be utilized for aggravating edge effects or defects in device structures. In the largest GOXCOMB structures (1000, 2000, and 4000 μm) the slots have been reduced to 5 μm, separated by 10 μm of field oxide, to further increase the aggravation caused by peripheral electric fields and edge-related defects.

It is anticipated that in most MOS process monitoring and development applications it would be possible to use wafers that had been previously patterned using the GASAD mask. Thus, the most important device structures would be complete after only one additional photolithographic step (see POLY, Section 4.4).

4.3 POLYCON

For most MOS monitoring or process development applications the POLYCON level would be omitted. The main reason for including this level has been to provide windows to the underlying GASAD tub diffusions or ion implantations that are required by the metallization test chip D (METEST). However, when investigation of p-n junctions with large areas or extended peripheries is required, the GASAD mask is used to define the diffused or ion-implanted regions. In this case the POLYCON level provides the required contact windows to junctions formed by the GASAD features. Evaluation of p-n junctions thus requires a minimum of three mask levels, because the POLY level must be used for metallization. If it should be necessary to investigate the effects of high-temperature processing after poly-Si deposition, such as oxidations and/or insulating depositions, additional mask levels WINDOW and METAL might be required.

4.4 POLY

It has been anticipated that the combination of GASAD followed by POLY would be the most widely used sequence of mask levels for MOS process development. For this reason, the POLY patterns have been extended to include the probing pads so that the poly-Si can be probed directly. Typical probe-spreading resistance measurements are of the order of 50Ω in a poly-Si film with a sheet resistance of 20 Ω/□, *providing that the probe tips are sufficiently hard and sharp enough to pierce* 50Å *of native oxide that typically occurs on the surface of* n^+*-poly-Si*. For this purpose tungsten carbide probes are recommended with tip radii of 5×10^{-4} cm or less. The use of palladium probes with planar tips 5×10^{-3} cm in diameter has been found to be unsatisfactory for probing n^+-poly-Si. Unfortunately, many probe cards designed for automatic probing cannot be used for probing n^+-poly-Si directly, because erratic probe contact resistance may range over many orders of magnitude, sometimes exceeding 10 megohms. Regular cleaning and inspection of probe tips are mandatory when probing n^+-poly-Si. Ion implantation causes an amorphous layer of semi-insulating material to occur near the surface of n^+-poly-Si. Thus, any n^+-poly-Si that has been exposed to ion implantation must be annealed at 950°C in N_2 for 30 minutes to avoid excessive probe resistance. In automatic probe stations with existing probe cards, the POLY mask level may be used to pattern aluminum, with or without an intervening poly-Si layer, to reduce probe resistance. Alternatively, the WINDOW and METAL mask levels can be used (see next sections).

At 200 μm and above, comb-like structures (POLYCOMB) are included in the POLY level for investigating edge effects or defects (see Fig. 4). The width and separation of individual elements are the same as for GOXCOMB (see GASAD, Section 4.2).

4.5 WINDOW

Occasionally, it is necessary to investigate changes in device characteristics resulting from oxidations, insulating depositions, or annealing after poly-Si definition. For this purpose the WINDOW level has been provided, which opens 90-μm square windows over each probing pad. In most cases the poly-Si could then be probed directly at the contact pads without resorting to aluminum deposition and lithography, providing the recommendations contained above in Section 4.4 are followed. In the case of the OVLAP and NOVLAP MOS capacitors surrounded by field plates, the capacitors must be probed directly. For this purpose, the WINDOW level also contains large contacting areas over each capacitor surrounded by a field plate. Occasionally, it may be beneficial to access the van der Pauw pattern with aluminum metallization. Therefore, the WINDOW level also contains four contacts oriented directly over the leads at the edges of the van der Pauw structures to provide conduction to overlying metal lines leading to the probing pads. The WINDOW level is also required for contacts to the sources and drains of IGFETs, the junction terminal of the GATODEs, and to SADSHEET.

4.6 METAL

As in the case of the GUARDRING and POLYCON levels, it is expected that the METAL level could be omitted in most MOS monitoring or process development applications. The principal exceptions include IGFETs and gated diodes, in which structures the required electrical continuity could not have been provided by the POLY level alone.

In most cases the metal has been excluded from any areas where poly-Si is in contact with gate oxide. The reason for this exclusion stems from experimental evidence that aluminum, sintered into polycrystalline silicon, sometimes deteriorates the dielectric breakdown strength of underlying gate oxides, especially if the gate oxide is very thin (i.e., ≤ 250Å). Exception occurs for all of the MOS capacitors surrounded by field plates, which must be probed directly. These OVLAP and NOVLAP capacitors thus provide experimental structures appropriate for cases in which it is necessary to compare the breakdown voltages in MOS capacitors with and without overlying metallization.

V. APPLICATIONS

Most basic circuit elements utilized by unipolar semiconductor integrated electronics can be easily fabricated with an appropriate subset of the lithographic mask system. These elements fall into five general classifications: MOS capacitors, p-n junctions, contacts, sheet resistors, and IGFETs. The contact class can be further subdivided to include guarded and unguarded Schottky diodes, ohmic contacts, and contact metallization test cells. The sheet resistor class can be subdivided to include polysilicon sheet resistors (POLYSHEET), source and drain sheet resistors (SADSHEET), and van der Pauw patterns in the GUARDRING, GASAD, and POLY levels. The IGFET class also includes gated diodes. These thirteen subdivisions of unipolar device structures are shown in the first column of Table VII. The remaining six columns show the *required* mask levels needed to realize a particular device structure. Other mask levels are generally optional, but some may be required for certain experiments.

At the present time the lithographic mask system is in wide use, and more than fifty experiments have been initiated in the Advanced Large-Scale Integration (LSI) Development Laboratory using one or more levels. References 22 through 26 contain published experiments that have utilized this mask system.

VI. SUMMARY

Fine-line MOS process characterization, determination of base-line parameters, and new process development can be efficiently carried out using the lithographic mask system. By selecting an appropriate subset of photo- or X-ray lithographic mask levels, most unipolar semiconductor circuit elements can be fabricated in an enormous range of sizes. X-ray and trilevel lithographic processes are used only when absolutely required, and these can be interleaved with photolithographically defined patterns. Any mask level can be aligned to any other, and any number of mask levels can be skipped. Registration tolerance is 5 μm for most device structures. Most experimental device structures can be completed and ready for electrical evaluation in a fraction of the time required to fabricate the elements on the Poon Tester chips,[1] which are included within the array of fine-line device chips and require six X-ray lithographic levels to complete.

VII. ACKNOWLEDGMENTS

The author is indebted to W. T. Lynch for initiating this project and for his continued interest, suggestions, and encouragement. The initial ideas were refined and implemented as a result of numerous discussions with E. N. Fuls, R. A. Kushner, E. I. Povilonis, and N. C. Wittwer. The universal alignment capability, resulting in modified PEP (MO-PEP) features, grew out of discussions with N. C. Wittwer, K. G. Schaffner, and R. Colish. The modification of X-ray alignment features to permit mixing of X-ray and photolithography was done by G. A. Coquin. The design of the metallization test chip (METEST) was carried out in collaboration with A. K. Sinha and S. Vaidya. Discussions with J. R. Brews and G. W. Taylor contributed to the design of the gated diodes and the option of buried channel capacitors. The TEM test chip was contributed by R. B. Marcus. Chip layouts were carried out by A. W. Russo, M. L. Oeser, J. P. Boyle, and M. Wagner of the Engineering Information Department. The wafer array was prepared by S. R. Juice, also of the Engineering Information Department. Mask fabrication was done in the Murray Hill Mask Lab; the cooperation of J. G. Skinner, L. J. Heilos, and other members of the Photomask and Pattern Generation Department is gratefully acknowledged. Final mask inspection was done by D. P. Rosenfeld of the Lithographic Systems Development Department.

Table I—Device key*

MOS Device	Nominal Dimension	Chip Assignment	Pad No(s).
HEXCAP Group			
1. FOXCAP	4000	C1	93
	2000	B	41
	1000	B	3
	500	A	2
	200	A	32
	100	A	26
	50	A	19
2. GOXCAP	4000	C1	42
	2000	B	49
	1000	B	7
	500	A	4
	200	A	31
	100	A	29
	50	A	20
	20	A	25
	15	A	1
	10	A	3
	7	A	5
	5	A	7
	4	A	8
	3	A	10
	2	A	11
	1.5	A	12
	1.0	A	14
3. GOXCOMB	4000	C2	67
	2000	B	106
	1000	B	34
	500	A	6
	200	A	30
4. POLYCOMB	4000	C3	68, 69, 70, 71
	2000	B	95, 96
	1000	B	22
	500	A	9
	200	A	29
5/6. OVLAP and NOVLAP with FIELD PLATE	4000	C4	14
	2000	B	75
	1000	B	13
	500	A	13
	200	A	33
	100	A	28
	50	A	18
SHEET Group			
1. SADSHEET	80SQ	A	15
	COM	A	16
	50SQ	A	17
2. POLYSHEET	80SQ	A	36
	COM	A	35
	50SQ	A	34
VANDERPAUW Group			
1. POLYSI	250	A	21
			22
			23
			24
2. GASAD	250	C4	101
			102
			103
			104
3. GUARDRING	250	C4	96
			97
			98
			99

* All dimensions are in micrometers. Exact areas and perimeters are listed in Tables II, III, and IV.

Table I—Device key*(*Continued*)

MOS Device	Nominal Dimension		Chip Assignment	Pad No(s).
4. POLYSI and GUARDRING	250		C4	87
				88
				89
				90
				91
				92
				93
				94
5. POLYSI and GASAD	250		C4	75
				76
				77
				78
				79
				80
				81
				82
IGFET Group	Channel			
Terminal	Width	Length		
1. Drain	100	20	B	87
	100	15	B	86
	100	10	B	85
	100	8	B	84
	100	6	B	83
	100	5	B	82
	100	4	B	81
	100	3	B	80
	100	2	B	79
	100	1.5	B	78
	100	1.0	B	77
Common Gate	100		B	88
Common Source	100		B	76
2. Source	500	500	B	53
Gate			B	54
Drain			B	55
3. Source	300	300	B	56
Gate			B	57
Drain			B	58
4. Source	200	200	B	59
Gate			B	60
Drain			B	61
5. Source	100	100	B	62
Gate			B	63
Drain			B	64
GATED DIODE Group	Channel			
Terminal	Width and Length			
1. Junction	500		B	65
Gate			B	67
2. Junction	300		B	68
Gate			B	69
3. Junction	200		B	70
Gate			B	71
4. Junction	100		B	72
Gate			B	73
METEST Group	Window Size			
1. Uni-Window	2		D	9–12
	3		D	3–6
	5		D	27–30
	7		D	21–24
2. Quad-Window	2		D	7, 8, 25, 26
3. Hex-Window	1.5		D	1, 2, 35, 36
4. Oct-Window	1		D	31–34

* All dimensions are in micrometers. Exact areas and perimeters are listed in Tables II, III, and IV.

Table II—Pad key for chip A *

Pad No.	MOS Device	Nom. Dim.	GASAD Area	GASAD Perimeter	POLYCON Area	POLY Area	POLY Perimeter	POLY Overlap FOX	POLY Overlap GOX	Window Area	Metal Area	GUARDRING (Width: 2) Area	GUARDRING (Width: 2) Perimeter	GUARDRING (Width: 2) Enclosed Area
1	GOXCAP	15	225	60	81	11,750	540	11,525	225	8,100	10,000	120	120	169
2	FOXCAP	500	0	0	0	271,350	2,490	271,350	0	8,100	10,000	262,144	2,048	0
3	GOXCAP	10	100	40	16	11,300	530	11,200	100	8,100	10,000	80	80	64
4	GOXCAP	500	250,000	2,000	100	271,350	2,490	21,350	250,000	8,100	10,000	4,000	4,000	248,004
5	GOXCAP	7	49	28	0	11,054	524	11,005	49	8,100	10,000	56	56	25
6	GOXCOMB	500	250,000	20,050	100	361,705	2,818	111,705	250,000	8,100	10,000	40,976	40,100	229,954
7	GOXCAP	5	25	20	0	10,900	520	10,875	25	8,100	10,000	40	40	9
8	GOXCAP	4	16	16	0	10,826	518	10,810	16	8,100	10,000	32	32	4
9	POLYCOMB	500	350,455	2,368	100	271,350	20,702	21,350	250,000	8,100	10,000	4,736	4,736	348,091
10	GOXCAP	3	9	12	0	10,754	516	10,745	9	8,100	10,000	24	24	1
11	GOXCAP	2	4	8	0	10,684	514	10,680	4	8,100	10,000	16	16	0
12	GOXCAP	1.5	2.25	6	0	10,649.75	513	10,647.5	2.25	8,100	10,000	12.25	14	0
13	FIELD PLATE	500	0	0	0	111,500	8,020	111,500	0	8,100	10,000	0	0	0
–	OVLAP	500	250,000	2,000	240,100	260,100	2,040	10,100	250,000	240,100	260,100	4,000	4,000	248,004
–	NOVLAP	500	260,100	2,040	240,100	250,000	2,000	0	250,000	240,100	250,000	4,080	4,080	258,064
14	GOXCAP	1.0	1.0	4	0	10,616	512	10,615	1.0	8,100	10,000	9	12	0
15	SADSHEET	80SQ	3,250	990	225	10,000	400	10,000	0	8,325	11,225	1,980	1,980	2,264
16	SADSHEET	COM			450	10,000	400	10,000	0	8,550	12,450			
17	SADSHEET	50SQ	4,450	984	225	10,000	400	10,000	0	8,325	11,225	1,968	1,968	3,470
18	FIELD PLATE	50	0	0	0	32,750	1,670	32,750	0	8,100	10,000	0	0	0
–	OVLAP	50	2,500	200	1,600	3,600	240	1,100	2,500	1,600	3,600	400	400	2,304
–	NOVLAP	50	3,600	240	1,600	2,500	200	0	2,500	1,600	2,500	480	480	3,364
19	FOXCAP	50	0	0	0	14,850	690	14,850	0	8,100	10,000	3,844	248	0
20	GOXCAP	50	2,500	200	100	14,850	690	12,350	2,500	8,100	10,000	400	400	2,304
21	VANDERPAUW	250	0	0	0	137,675	5,210	137,675	0	8,685	30,912.5	63,504	1,008	0
22	VANDERPAUW	250	0	0	0	137,675	5,210	137,675	0	8,587.5	15,587.5	63,504	1,008	0
23	VANDERPAUW	250	0	0	0	137,675	5,210	137,675	0	8,437.5	11,212.5	63,504	1,008	0
24	VANDERPAUW	250	0	0	0	137,675	5,210	137,675	0	8,602.5	17,462.5	63,504	1,008	0
25	GOXCAP	20	400	80	100	12,250	550	11,850	400	8,100	10,000	160	160	324
26	FOXCAP	100	0	0	0	23,350	890	23,350	0	8,100	10,000	12,544	448	0
27	GOXCAP	100	10,000	400	100	23,350	890	13,350	10,000	8,100	10,000	800	800	9,604
28	FIELD PLATE	100	0	0	0	37,750	2,520	37,750	0	8,100	10,000	0	0	0
–	OVLAP	100	10,000	400	8,100	12,100	440	2,100	10,000	8,100	12,100	800	800	9,604
–	NOVLAP	100	12,100	440	8,100	10,000	400	0	10,000	8,100	10,000	880	880	11,664
29	POLYCOMB	200	56,350	950	100	55,350	3,782	15,350	40,000	8,100	10,000	1,900	1,900	55,404
30	GOXCOMB	200	40,000	3,250	100	67,600	1,400	27,600	40,000	8,100	10,000	6,500	6,472	36,754
31	GOXCAP	200	40,000	800	100	55,350	1,290	15,350	40,000	8,100	10,000	1,600	1,600	39,204
32	FOXCAP	200	0	0	0	55,350	1,290	55,350	0	8,100	10,000	44,944	848	0
33	FIELD PLATE	200	0	0	0	56,787.5	4,043	56,787.5	0	8,100	10,000	0	0	0
–	OVLAP	200	40,000	800	36,100	44,100	840	4,100	40,000	36,100	44,100	1,600	1,600	39,204
–	NOVLAP	200	44,100	840	36,100	40,000	800	0	40,000	36,100	40,000	1,680	1,680	43,264
34	POLYSHEET	50SQ	0	0	0				0	8,100	10,000	4,020	814	0
35	POLYSHEET	COM	0	0	0	35,216	2,778	35,216	0	8,100	10,000			
36	POLYSHEET	80SQ	0	0	0				0	8,100	10,000	2,800	824	0

* All dimensions are in micrometers.

Table II—Pad key for chip A* (*Continued*)

PAD No.	MOS device	Nom. Dim.	GUARDRING (Width: 3)			GUARDRING (Width: 5)			GUARDRING (Width: 7)			GUARDRING (Width: 10)		
			Area	Peri-meter	Enclosed Area	Area	Peri-meter	Enclosed Area	Area	Peri-meter	Enclosed Area	Area	Peri-meter	Enclosed Area
1	GOXCAP	15	180	120	144	300	120	100	420	120	64	600	120	25
2	FOXCAP	500	263,169	2,052	0	265,225	2,060	0	267,289	2,068	0	270,400	2080	0
3	GOXCAP	10	120	80	49	200	80	25	280	80	9	400	80	0
4	GOXCAP	500	6,000	4,000	247,009	10,000	4,000	245,025	14,000	4,000	243,049	20,000	4,000	240,100
5	GOXCAP	7	84	56	16	140	56	4	196	56	0	289	68	0
6	GOXCOMB	500	60,150	40,100	219,934	100,250	40,100	199,900	140,350	40,100	179,874	200,560	22,404	149,850
7	GOXCAP	5	60	40	4	100	40	0	144	48	0	225	60	0
8	GOXCAP	4	48	32	1	81	36	0	121	44	0	196	56	0
9	POLYCOMB	500	7,104	4,736	346,912	11,840	4,736	344,560	16,576	4,736	342,216	23,680	4,736	338,715
10	GOXCAP	3	36	24	0	64	32	0	100	40	0	169	52	0
11	GOXCAP	2	25	20	0	49	28	0	81	36	0	144	48	0
12	GOXCAP	1.5	20.25	18	0	42.25	26	0	72.25	34	0	132.25	46	0
13	FIELD PLATE	500	0	0	0	0	0	0	0	0	0	0	0	0
—	OVLAP	500	6,000	4,000	247,009	10,000	4,000	245,025	14,000	4,000	243,049	20,000	4,000	240,100
—	NOVLAP	500	6,120	4,080	257,049	10,200	4,080	255,025	14,280	4,080	253,009	20,400	4,080	250,000
14	GOXCAP	1.0	16	16	0	36	24	0	64	32	0	121	44	0
15	SADSHEET	80SQ	2,970	1,980	1,774	4,950	1,090	800	6,130	1,090	648	7,850	1,150	450
16	SADSHEET	COM												
17	SADSHEET	50SQ	2,952	1,968	2,983	4,920	1,968	2,015	6,888	1,968	1,055	9,020	1,024	450
18	FIELD PLATE	50	0	0	0	0	0	0	0	0	0	0	0	0
—	OVLAP	50	600	400	2,209	1,000	400	2,025	1,400	400	1,849	2,000	400	1,600
—	NOVLAP	50	720	480	3,249	1,200	480	3,025	1,680	480	2,809	2,400	480	2,500
19	FOXCAP	50	3,969	252	0	4,225	260	0	4,489	268	0	4,900	280	0
20	GOXCAP	50	600	400	2,209	1,000	400	2,025	1,400	400	1,849	2,000	400	1,600
21	VANDERPAUW	250	64,009	1,012	0	65,025	1,020	0	66,049	1,028	0	67,600	1,040	0
22	VANDERPAUW	250	64,009	1,012	0	65,025	1,020	0	66,049	1,028	0	67,600	1,040	0
23	VANDERPAUW	250	64,009	1,012	0	65,025	1,020	0	66,049	1,028	0	67,600	1,040	0
24	VANDERPAUW	250	64,009	1,012	0	65,025	1,020	0	66,049	1,028	0	67,600	1,040	0
25	GOXCAP	20	240	160	289	400	160	225	560	160	169	800	160	100
26	FOXCAP	100	12,769	452	0	13,225	460	0	13,689	468	0	14,400	480	0
27	GOXCAP	100	1,200	800	9,409	2,000	800	9,025	2,800	800	8,649	4,000	800	8,100
28	FIELD PLATE	100	0	0	0	0	0	0	0	0	0	0	0	0
—	OVLAP	100	1,200	800	9,409	2,000	800	9,025	2,800	800	8,649	4,000	800	8,100
—	NOVLAP	100	1,320	880	11,449	2,200	880	11,025	3,080	880	10,609	4,400	880	10,000
29	POLYCOMB	200	2,850	1,900	54,934	4,750	1,900	54,000	6,650	1,900	53,074	9,500	1,900	51,700
30	GOXCOMB	200	9,360	6,458	35,134	16,250	6,430	31,900	22,750	28,674	6,402	55,200	4,120	23,850
31	GOXCAP	200	2,400	1,600	38,809	4,000	1,600	38,025	5,600	1,600	37,249	8,000	1,600	36,100
32	FOXCAP	200	45,369	852	0	46,225	860	0	47,089	868	0	48,400	880	0
33	FIELD PLATE	200	0	0	0	0	0	0	0	0	0	0	0	0
—	OVLAP	200	2,400	1,600	38,809	4,000	1,600	38,025	5,600	1,600	37,249	8,000	1,600	36,100
—	NOVLAP	200	2,520	1,680	42,849	4,200	1,680	42,025	5,880	1,680	41,209	8,400	1,680	40,000
34	POLYSHEET	50SQ	4,422	826	0	5,226	830	0	6,030	834	0	7,236	840	0
35	POLYSHEET	COM												
36	POLYSHEET	80SQ	3,200	816	0	4,000	820	0	4,800	824	0	6,000	830	0

* All dimensions are in micrometers.

Table III—Pad key for chip B*

Pad No.	MOS Device	Nom. Dim.	GASAD Area	GASAD Perimeter	POLYCON Area	POLY Area	POLY Perimeter	POLY Overlap FOX	POLY Overlap GOX	Window Area	Metal Area	GUARDRING (Width: 2) Area	GUARDRING (Width: 2) Perimeter	GUARDRING (Width: 2) Enclosed Area
3	FOXCAP	1,000	0	0	0	1,031,350	4,490	1,031,350	0	8,100	10,000	1,024,144	4,048	0
7	GOXCAP	1,000	1,000,000	4,000	100	1,031,350	4,490	31,350	1,000,000	8,100	10,000	8,000	8,000	996,004
13	FIELD PLATE	1,000	0	0	0	209,000	15,170	209,000	0	8,100	10,000	0	0	0
–	OVLAP	1,000	1,000,000	4,000	980,100	1,020,100	4,040	20,100	1,000,000	980,100	1,020,100	8,000	8,000	996,004
–	NOVLAP	1,000	1,020,100	4,040	980,100	1,000,000	4,000	0	1,000,000	980,100	1,000,000	8,080	8,080	1,016,064
22	POLYCOMB	1,000	2,027,970	5,766	90	706,350	270,927	31,325	675,025	8,100	10,000	11,532	11,532	2,022,208
34	GOXCOMB	1,000	675,000	270,020	90	2,038,220	6,256	1,363,220	675,000	8,100	10,000	540,020	540,020	404,994
41	FOXCAP	2,000	0	0	0	4,051,350	8,490	4,051,350	0	8,100	10,000	4,048,144	8,048	0
49	GOXCAP	2,000	4,000,000	8,000	100	4,051,350	8,490	51,350	4,000,000	8,100	10,000	16,000	16,000	3,992,004
53	IGFET: SOURCE		0	0	0					10,500	18,250	1,080	1,084	0
54	IGFET: GATE	500	275,000	2,100	0	265,500	2,500	15,500	250,000	8,100	10,000			
55	IGFET: DRAIN				0					10,500	18,250	1,080	1,084	0
56	IGFET: SOURCE		0	0	0					9,500	18,647.5	680	684	0
57	IGFET: GATE	300	105,000	1,300	0	103,500	1,700	13,500	90,000	8,100	10,000			
58	IGFET: DRAIN				0					9,500	18,647.5	680	684	0
59	IGFET: SOURCE				0					9,000	16,487.5	480	484	0
60	IGFET: GATE	200	50,000	900	0	52,500	1,300	12,500	40,000	8,100	10,000			
61	IGFET: DRAIN				0					9,000	16,487.5	480	484	0
62	IGFET: SOURCE				0					8,500	14,987.5	280	284	0
63	IGFET: GATE	100	15,000	500	0	21,500	900	11,500	10,000	8,100	10,000			
64	IGFET: DRAIN				0					8,500	14,987.5	280	284	0
65	GATOD: JUNC.	500	278,200	2,110	0					10,600	18,475	4,220	4,220	276,094
67	GATOD: GATE				0	263,475	2,517	13,375	250,100	8,100	10,000			
68	GATOD: JUNC.	300	107,200	1,310	0					9,600	15,475	2,620	2,620	105,894
69	GATOD: GATE				0	102,350	1,672	12,250	90,100	8,100	10,000			
70	GATOD: JUNC.	200	51,700	910	0					9,100	13,975	1,820	1,820	50,794
71	GATOD: GATE				0	52,190	1,618	12,090	40,100	8,100	10,000			
72	GATOD: JUNC.	100	16,200	510	0					8,100	8,600	1,020	1,020	15,694
73	GATOD: GATE				0	21,600	1,100	11,500	10,100	8,100	10,000			
75	FIELD PLATE	2,000	0	0	0	436,500	30,220	436,500	0	8,100	10,000	0	0	0
–	OVLAP	2,000	4,000,000	8,000	3,960,100	4,040,100	8,040	40,100	4,000,000	3,960,100	4,040,100	16,000	16,000	3,992,004
–	NOVLAP	2,000	4,040,100	8,040	3,960,100	4,000,000	8,000	0	4,000,000	3,960,100	4,000,000	16,080	16,080	4,032,064
76	IGFET: COMSOURCE		0	0	0	10,000	400	10,000	0	12,500	61,100	280	284	0
77	IGFET: DRAIN	1.0	5,100	302	0	10,000	400	10,000	0	8,500	16,935			
78	IGFET: DRAIN	1.5	5,150	303	0	10,000	400	10,000	0	8,500	16,875			
79	IGFET: DRAIN	2	5,200	304	0	10,000	400	10,000	0	8,500	16,870			
80	IGFET: DRAIN	3	5,300	306	0	10,000	400	10,000	0	8,500	16,820			
81	IGFET: DRAIN	4	5,400	308	0	10,000	400	10,000	0	8,500	16,770			
82	IGFET: DRAIN	5	5,500	310	0	10,000	400	10,000	0	8,500	16,720			
83	IGFET: DRAIN	6	5,600	312	0	10,000	400	10,000	0	8,500	16,670			
84	IGFET: DRAIN	8	5,800	316	0	10,000	400	10,000	0	8,500	16,565			
85	IGFET: DRAIN	10	6,000	320	0	10,000	400	10,000	0	8,500	16,465			
86	IGFET: DRAIN	15	6,500	330	0	10,000	400	10,000	0	8,500	16,225			
87	IGFET: DRAIN	20	7,000	340	0	10,000	400	10,000	0	8,500	15,980			
88	IGFET: COMGATE		0	0	0	31,650	5,595	24,100	7,550	8,100	10,000	280	284	0
95	POLYCOMB	2,000	8,028,720	11,334	90	2,717,840	1,072,598	51,350	2,666,490	8,100	10,000	22,668	22,668	8,017,390
106	GOXCOMB	2,000	2,676,190	1,070,486	90	8,038,970	11,824	5,362,780	2,676,190	8,100	10,000	2,140,972	2,140,972	1,605,708

* All dimensions are in micrometers.

Table III—Pad key for chip B* (*Continued*)

PAD No.	MOS Device	Nom. Dim.	GUARDRING (Width: 3)			GUARDRING (Width: 5)			GUARDRING (Width: 7)			GUARDRING (Width: 10)		
			Area	Peri-meter	Enclosed Area	Area	Peri-meter	Enclosed Area	Area	Peri-meter	Enclosed Area	Area	Peri-meter	Enclosed Area
3	FOXCAP	1,000	1,026,169	4,052	0	1,030,225	4,060	0	1,034,289	4,068	0	1,040,400	4,080	0
7	GOXCAP	1,000	12,000	8,000	994,009	20,000	8,000	990,025	28,000	8,000	986,049	40,000	8,000	980,100
13	FIELD PLATE	1,000	0	0	0	0	0	0	0	0	0	0	0	0
—	OVLAP	1,000	12,000	8,000	994,009	20,000	8,000	990,025	28,000	8,000	986,049	40,000	8,000	980,100
—	NOVLAP	1,000	12,120	8,080	1,014,049	20,200	8,080	1,010,025	28,280	8,080	1,006,009	40,400	8,080	1,000,000
22	POLYCOMB	1,000	17,298	11,532	2,019,330	28,830	11,532	2,013,580	40,362	11,532	2,007,838	57,660	11,532	1,999,240
34	GOXCOMB	1,000	810,030	540,020	269,994	2,013,580	5,746	0	2,019,330	5,754	0	2,027,970	5,766	0
41	FOXCAP	2,000	4,052,169	8,052	0	4,060,225	8,060	0	4,068,289	8,068	0	4,080,400	8,080	0
49	GOXCAP	2,000	24,000	16,000	3,988,009	40,000	16,000	3,980,025	56,000	16,000	3,972,049	80,000	16,000	3,960,100
53	IGFET: SOURCE		1,620	1,086	0	2,700	1,090	0	3,780	1,094	0	5,400	1,100	0
54	IGFET: GATE	500												
55	IGFET: DRAIN		1,620	1,086	0	2,700	1,090	0	3,780	1,094	0	5,400	1,100	0
56	IGFET: SOURCE		1,020	686	0	1,700	690	0	2,380	694	0	3,400	700	0
57	IGFET: GATE	300												
58	IGFET: DRAIN		1,020	686	0	1,700	690	0	2,380	694	0	3,400	700	0
59	IGFET: SOURCE		720	486	0	1,200	490	0	1,680	494	0	2,400	500	0
60	IGFET: GATE	200												
61	IGFET: DRAIN		720	486	0	1,200	490	0	1,680	494	0	2,400	500	0
62	IGFET: SOURCE		420	286	0	700	290	0	980	294	0	1,400	300	0
63	IGFET: GATE	100												
64	IGFET: DRAIN		420	286	0	700	290	0	980	294	0	1,400	300	0
65	GATOD: JUNC.	500	6,330	4,220	275,044	10,550	4,220	272,950	14,770	4,220	270,864	21,100	4,220	267,750
67	GATOD: GATE													
68	GATOD: JUNC.	300	3,930	2,620	105,244	6,550	2,620	103,950	9,170	2,620	102,664	13,100	1,620	100,750
69	GATOD: GATE													
70	GATOD: JUNC.	200	2,730	1,820	50,344	4,550	1,820	49,450	6,370	1,820	48,564	9,100	1,820	47,250
71	GATOD: GATE													
72	GATOD: JUNC.	100	1,530	1,020	15,444	2,550	1,020	14,950	3,570	1,020	14,464	5,100	1,020	13,750
73	GATOD: GATE													
75	FIELD PLATE	2,000	0	0	0	0	0	0	0	0	0	0	0	0
—	OVLAP	2,000	24,000	16,000	3,988,009	40,000	16,000	3,980,025	56,000	16,000	3,972,049	80,000	16,000	3,960,100
—	NOVLAP	2,000	24,120	16,080	4,028,049	40,200	16,080	4,020,025	56,280	16,080	4,012,009	80,400	16,080	4,000,000
76	IGFET: COMSOURCE		420	286	0	700	290	0	980	294	0	1,400	300	0
77	IGFET: DRAIN	1.0												
78	IGFET: DRAIN	1.5												
79	IGFET: DRAIN	2												
80	IGFET: DRAIN	3												
81	IGFET: DRAIN	4												
82	IGFET: DRAIN	5												
83	IGFET: DRAIN	6												
84	IGFET: DRAIN	8												
85	IGFET: DRAIN	10												
86	IGFET: DRAIN	15												
87	IGFET: DRAIN	20												
88	COMGATE		420	286	0	700	290	0	980	294	0	1,400	300	0
95	POLYCOMB	2,000	34,002	22,668	8,011,728	56,670	22,668	8,000,410	79,338	22,668	7,989,100	113,340	22,668	7,972,150
106	GOXCOMB	2,000	3,211,458	2,140,972	1,070,470	8,000,410	11,314	0	8,011,728	11,322	0	8,028,720	11,334	0

* All dimensions are in micrometers.

Table IV—Pad key for chips C1 through C4 *

Pad No.	MOS Device	Chip	Nom. Dim.	GASAD Area	GASAD Perimeter	Polycon Area	POLY Area	POLY Perimeter	POLY Overlap FOX	POLY Overlap GOX	Window Area	Metal Area	GUARDING (Width: 10) Area	GUARDING Perimeter	GUARDING Enclosed Area
42	GOXCAP	C1	4,000	16,000,000	16,400	100	16,093,350	16,890	93,350	16,000,000	8,100	10,000	164,000	32,800	15,918,100
43	FOXCAP	C1	4,000	0	0	0	16,093,350	16,890	16,093,350	0	8,100	10,000	16,164,400	16,480	0
67	GOXCOMB	C2	4,000	14,400,000	5,760,010	90	43,221,500	27,020	28,821,500	14,400,000	8,100	10,000	43,211,250	26,530	0
68-71	POLYCOMB	C3	4,000	43,211,250	26,530	90	14,493,350	5,762,167	93,350	14,400,000	32,400	40,000	265,300	53,060	43,078,700
14	FIELD PLATE	C4	4,000	0	0	0	715,500	56,600	715,500	0	8,100	10,000	0	0	0
–	OVLAP	C4	4,000	16,000,000	16,400	15,918,100	16,082,100	16,440	82,100	16,000,000	15,918,100	16,082,100	164,000	32,800	15,918,100
–	NOVLAP	C4	4,000	16,082,100	16,440	15,918,100	16,000,000	16,400	0	16,000,000	15,918,100	16,000,000	164,400	32,880	16,000,000
	DOUBLE VANDERPAUW														
75	GASAD	C4	250	67,812.5	1,425	585.0	53,252.5	3,865			8,685.0	43,382.5	0	0	0
76	POLY	C4	260	0	0	0	169,975	7,430	101,875	68,100	8,685.0	34,675.0	0	0	0
77	GASAD	C4	250	67,812.5	1,425	487.5	29,597.5	1,971			8,587.5	19,715.0	0	0	0
78	POLY	C4	260	0	0	0	169,975	7,430	101,875	68,100	8,587.5	13,125.0	0	0	0
79	GASAD	C4	250	67,812.5	1,425	337.5	15,077.5	811			8,437.5	5,202.5	0	0	0
80	POLY	C4	260	0	0	0	169,975	7,430	101,875	68,100	8,437.5	3,062.5	0	0	0
81	GASAD	C4	250	67,812.5	1,425	502.5	16,952.5	961			8,602.5	7,072.5	0	0	0
82	POLY	C4	260	0	0	0	169,975	7,430	101,875	68,100	8,602.5	15,325.0	0	0	0
87	GUARDRING	C4	250	0	0	585.0	55,600	4,048	55,600	0	8,685.0	55,725	67,812.5	1,425	0
88	POLY	C4	260	0	0	0	172,875	7,662	172,875	0	8,685.0	43,875	0	0	0
89	GUARDRING	C4	250	0	0	487.5	29,425	1,954	29,425	0	8,587.5	29,550	67,812.5	1,425	0
90	POLY	C4	260	0	0	0	172,875	7,662	172,875	0	8,587.5	23,550	0	0	0
91	GUARDRING	C4	250	0	0	337.5	14,300	794	14,300	0	8,437.5	14,425	67,812.5	1,425	0
92	POLY	C4	260	0	0	0	172,875	7,662	172,875	0	8,437.5	11,675	0	0	0
93	GUARDRING	C4	250	0	0	502.5	16,800	944	16,800	0	8,602.5	16,925	67,812.5	1,425	0
94	POLY	C4	260	0	0	0	172,875	7,662	172,875	0	8,602.5	26,675	0	0	0
	VANDERPAUW														
96	GUARDRING	C4	250	0	0	585.0	31,350	2,108	31,350	0	8,685.0	31,325	67,225	1,378	0
97	GUARDRING	C4	250	0	0	487.5	16,025	882	16,025	0	8,587.5	16,025	67,225	1,378	0
98	GUARDRING	C4	250	0	0	337.5	11,650	532	11,650	0	8,437.5	11,650	67,225	1,378	0
99	GUARDRING	C4	250	0	0	502.5	17,900	1,032	17,900	0	8,602.5	17,900	67,225	1,378	0
101	GASAD	C4	250	67,075	1,366	585.0	31,387.5	2,111	30,087.5	1,300.0	8,685.0	31,387.5	0	0	0
102	GASAD	C4	250	67,075	1,366	487.5	16,062.5	885	14,875.0	1,187.5	8,587.5	16,062.5	0	0	0
103	GASAD	C4	250	67,075	1,366	337.5	11,687.5	535	10,775.0	912.5	8,437.5	11,687.5	0	0	0
104	GASAD	C4	250	67,075	1,366	502.5	17,937.5	1,035	16,762.5	1,175.0	8,602.5	17,937.5	0	0	0

* All dimensions are in micrometers.

Table V—Pad key for METEST chip D*

PAD NO.	GASAD			POLYCON			POLY							
	TUB			WINDOW			TAPS			TIES			CONTACTS	
	SIZE	NO.	AREA	SIZE	NO.	AREA†	W_1	L_1	SQ_1	W_2	L_2	SQ_2	W_3	L_3
1,2	20×78	4	6,240	1.5	6	13.5	25	187	7.48	5	50	10	11.5	272
3,4	20×36	2	1,440	3	1	9	25	125	5	5	153	30.6	13	52
4,5	20×36	1	720	3	1	9	25	125	5	5	189	37.8	13	26
5,6	20×36	4	2,880	3	1	9	25	125	5	5	81	16.2	13	104
7,26	20×70	4	5,600	2	4	16	25	125	5	5	746.5	149.3	12	240
7,8	20×70	7	9,800	2	4	16	25	125	5	5	1788.0	357.6	12	420
8,25	20×70	2	2,800	2	4	16	25	125	5	5	886.5	177.3	12	120
9,10	20×34	2	1,360	2	1	4	25	125	5	5	157	31.4	12	48
10,11	20×34	1	680	2	1	4	25	125	5	5	191	38.2	12	24
11,12	20×34	4	2,720	2	1	4	25	125	5	5	89	17.8	12	96
13,14	20×33	2	1,320	1.5	1	2.25	25	125	5	5	159	31.8	11.5	46
14,15	20×33	1	660	1.5	1	2.25	25	125	5	5	222	44.4	11.5	23
15,16	20×33	4	2,640	1.5	1	2.25	25	125	5	5	93	18.6	11.5	92
17,18	20×32	2	1,280	1.0	1	1	25	125	5	5	161	32.2	11	44
18,19	20×32	1	640	1.0	1	1	25	125	5	5	223	44.6	11	22
19,20	20×32	4	2,560	1.0	1	1	25	125	5	5	97	19.4	11	88
21,22	20×44	2	1,760	7	1	49	25	125	5	5	137	27.4	17	68
22,23	20×44	1	880	7	1	49	25	125	5	5	181	36.2	17	34
23,24	20×44	4	3,520	7	1	49	25	125	5	5	49	9.8	17	136
25,26	20×70	1	1,400	2	4	16	25	125	5	5	155	31	12	60
27,28	20×40	2	1,600	5	1	25	25	125	5	5	145	29	15	60
28,29	20×40	1	800	5	1	25	25	125	5	5	185	37	15	30
29,30	20×40	4	3,200	5	1	25	25	125	5	5	65	13	15	120
31,32	20×74	2	2,960	1.0	8	8	25	125	5	5	77	15.4	11	128
32,33	20×74	1	1,480	1.0	8	8	25	125	5	5	143.5	28.7	11	64
33,34	20×74	4	5,920	1.0	8	8	25	171	6.84	5	50	10	11	256
35,36	20×78	2	3,120	1.5	6	13.5	25	125	5	5	69	13.8	11.5	136
36,1	20×78	1	1,560	1.5	6	13.5	25	125	5	5	139.5	27.9	11.5	68

* All dimensions are in micrometers.
† Cross-sectional area of tub input or output.

Table VI—Mask levels

Suggested Sequence	Mask Level	Tone	Note	Features	Background
1	GUARDRING	Normal	1	Clear	Opaque
2	GASAD	Normal	1	Clear	Opaque
3	POLYCON	Normal	1	Clear	Opaque
4	POLY	Normal	1	Opaque	Clear
5	WINDOW	Normal	1	Clear	Opaque
6	METAL	Normal	1	Opaque	Clear
$\overline{2}$	R. T. GASAD	Reverse	2	Opaque	Clear
$\overline{4}$	R. T. POLY	Reverse	2	Clear	Opaque
$\overline{6}$	R. T. METAL	Reverse	2	Clear	Opaque

1. For use with positive photoresist.
2. For use with negative photoresist, uniform gold metallization, selective oxidation, or other special processes.

Table VII—Experimental devices

Device Structures		GUARDRING	GASAD	POLYCON	POLY	WINDOW	METAL
		Required Mask Levels					
MOS Capacitors			*		*		
Schottky Diodes:	Guarded	*	*		*		
	Unguarded		*		*		
Ohmic Contacts			*	*	*		
p-n Junctions			*	*	*		
IGFETs			*		*	*	*
Gated Diodes	GATODE		*		*	*	*
SADSHEET			*			*	*
POLYSHEET					*		
VANDERPAUW:	POLY				*		
	GASAD		*	*	*		
	GUARDRING	*		*	*		
Contact Metallization Test Cells	METEST		*	*	*		

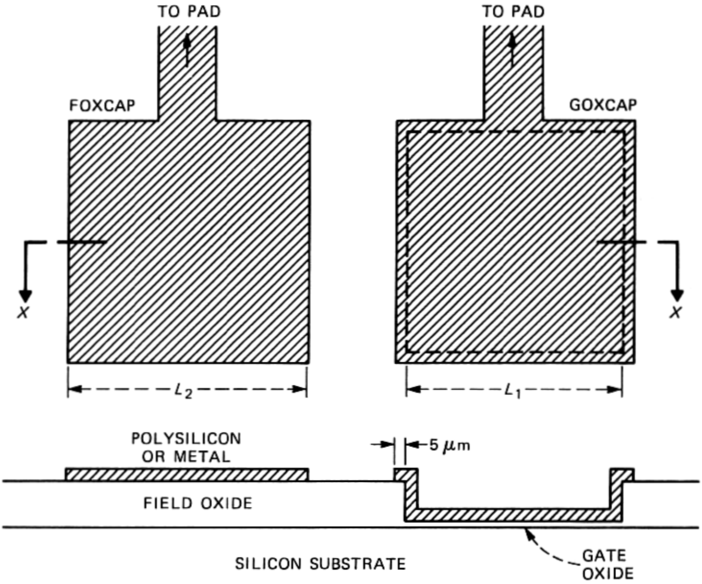


Fig. 1—FOXCAP and GOXCAP MOS capacitors (chips A through C).

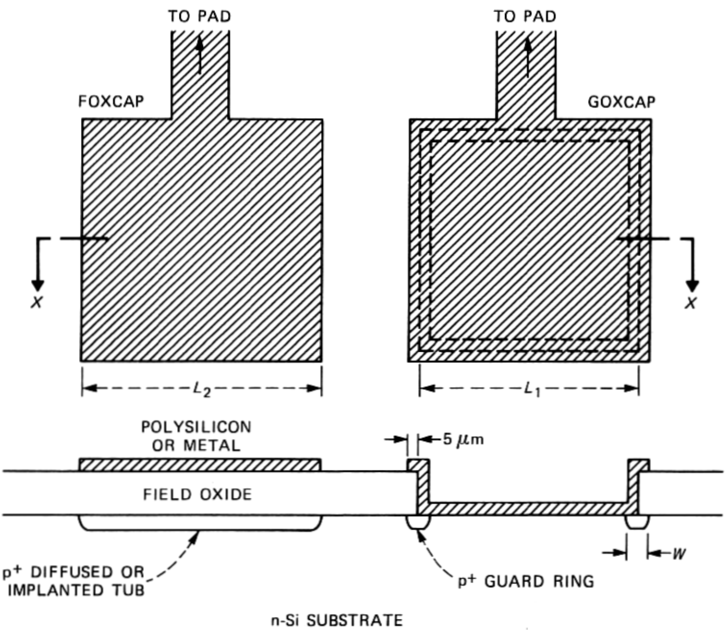


Fig. 2—Guarded Schottky diode and buried channel capacitor formed with FOXCAP and GOXCAP features (chips A through C).

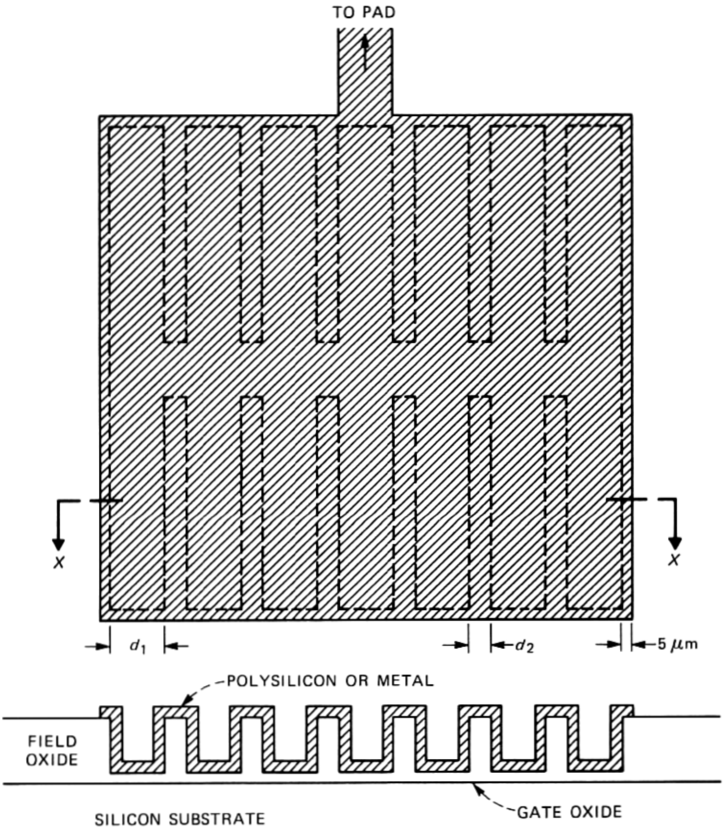


Fig. 3—GOXCOMB MOS capacitor (chips A through C).

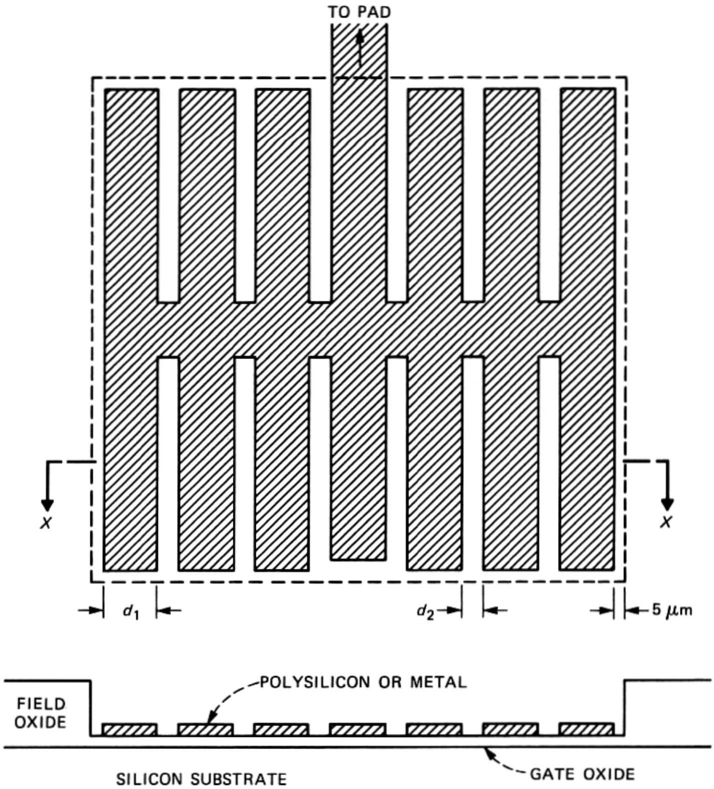


Fig. 4—POLYCOMB MOS capacitor (chips A through C).

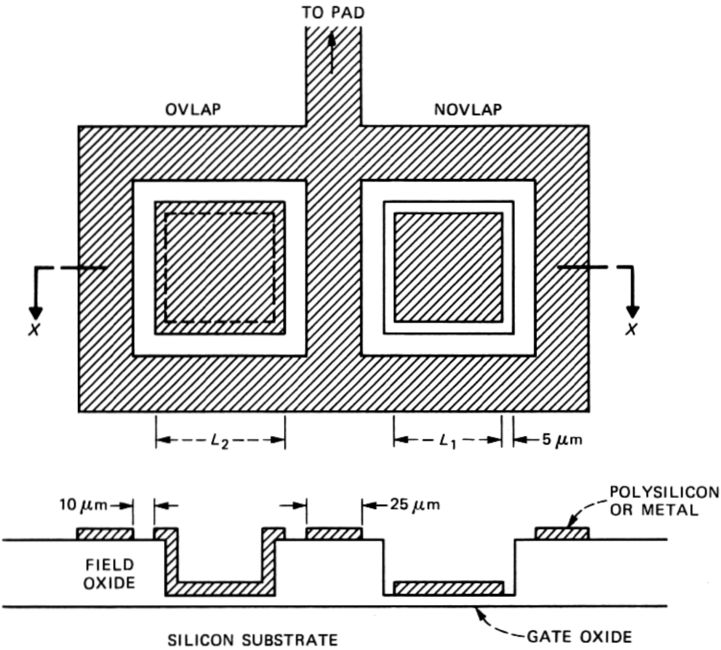


Fig. 5—OVLAP and NOVLAP MOS capacitors with field plate to control surrounding surface potential (chips A through C).

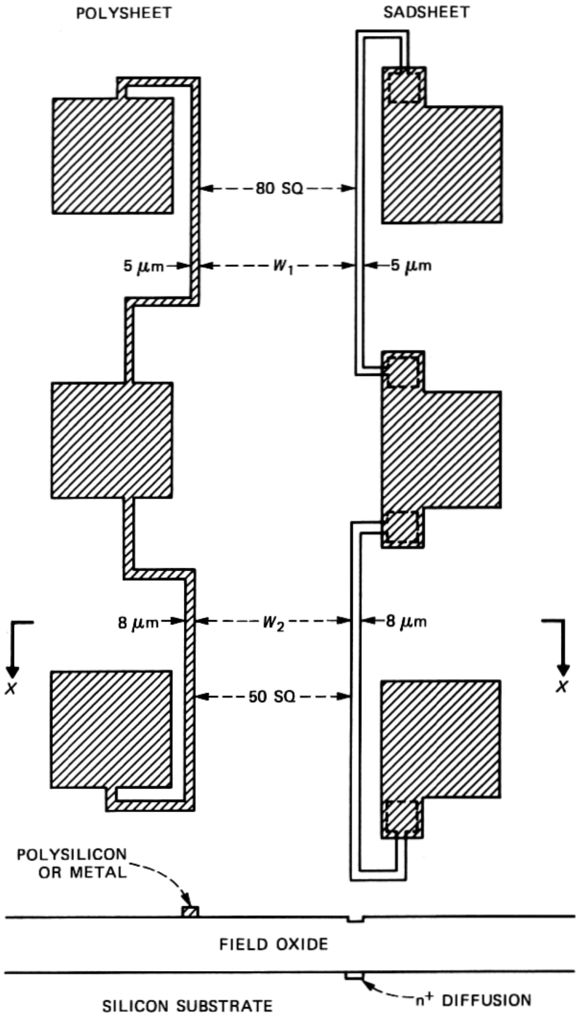


Fig. 6—POLYSHEET and SADSHEET sheet resistance and linewidth features (chip A).

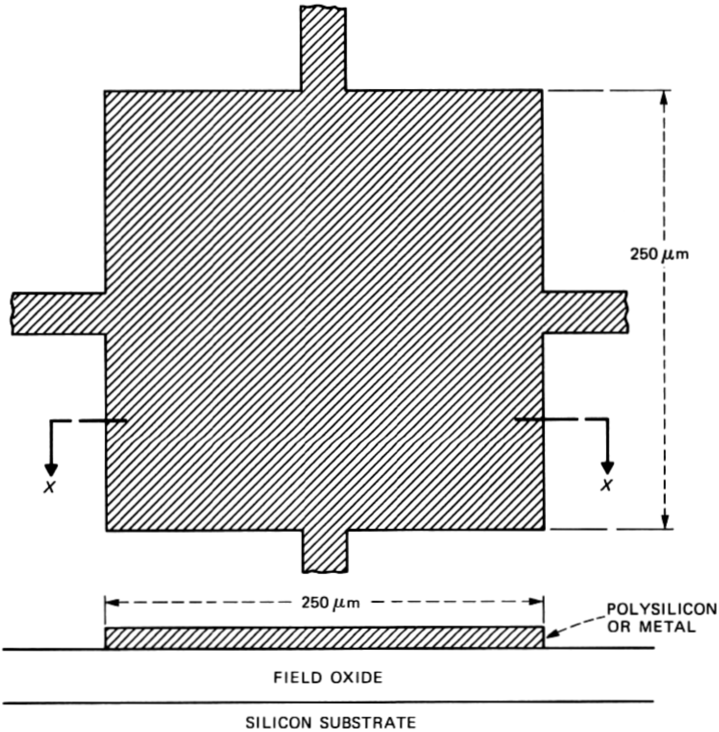


Fig. 7—Van der Pauw pattern (chip A and chip C4).

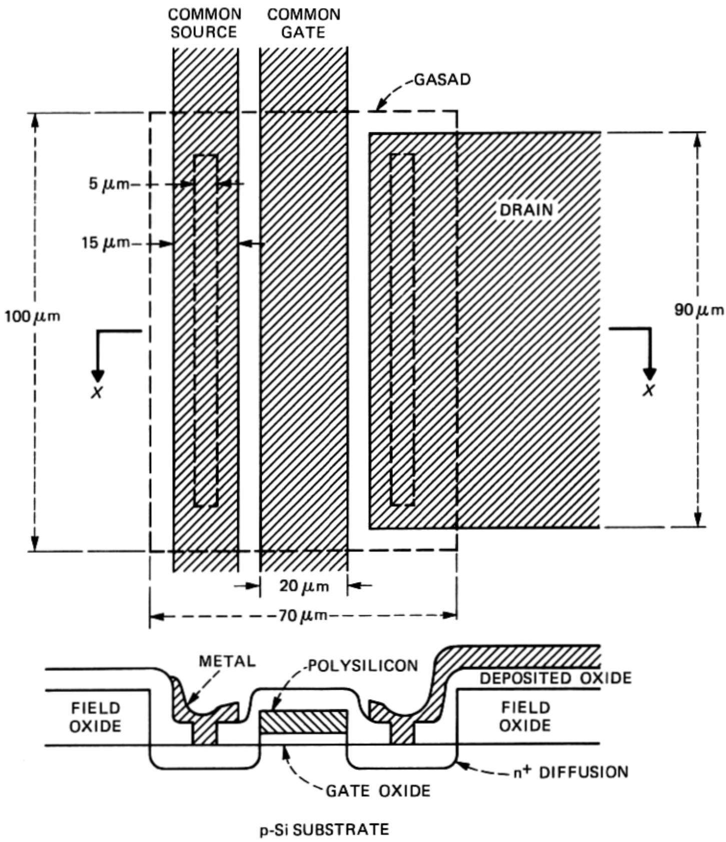


Fig. 8—Standard IGFET with common sources and drains (chip B).

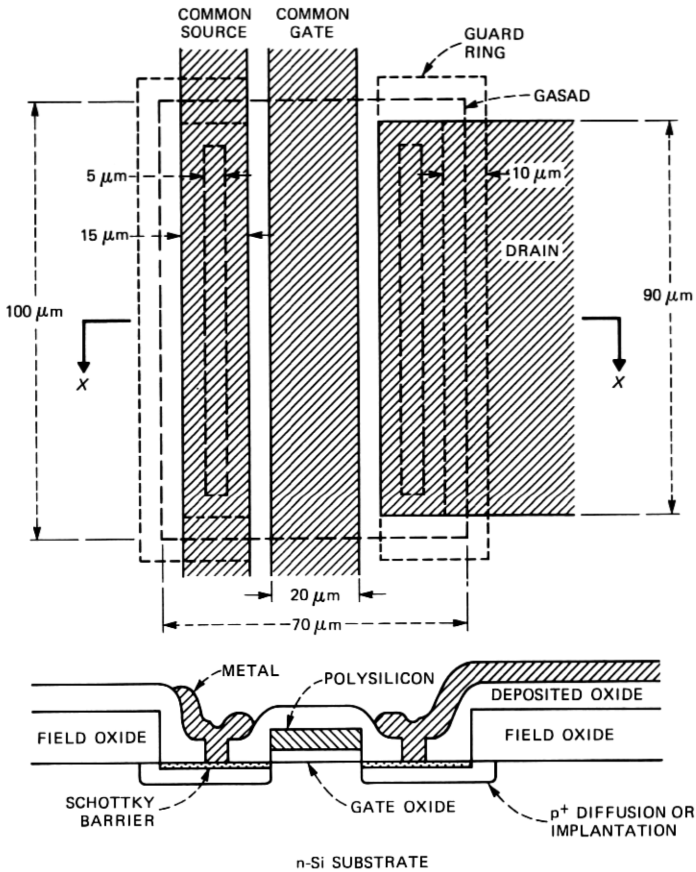


Fig. 9—Guarded IGFET with common sources and drains (chip B).

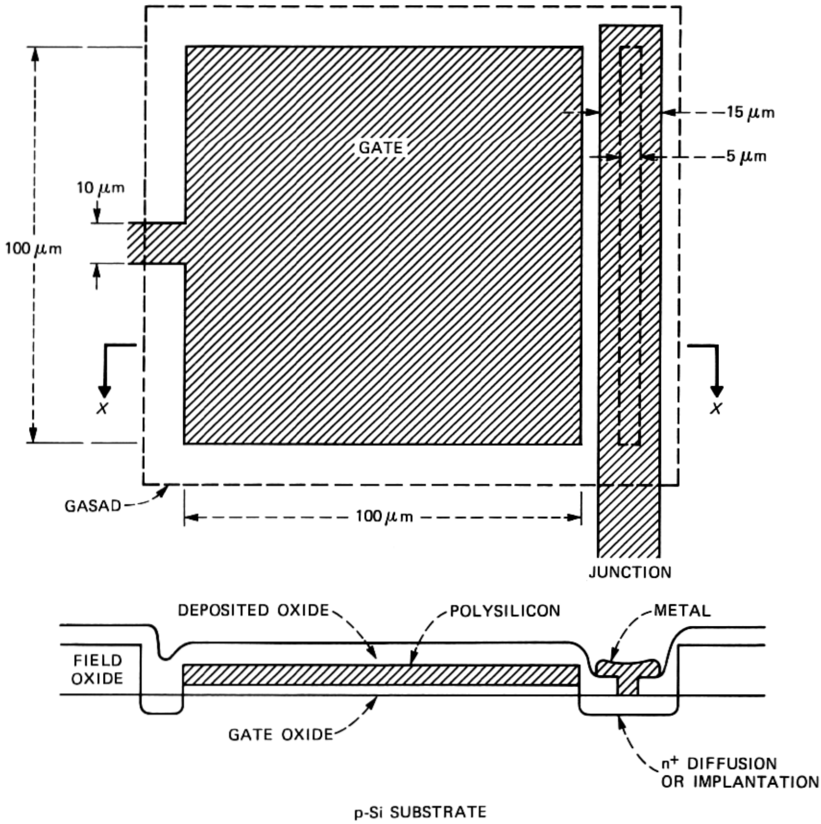


Fig. 10—Gated diode with n^+ diffusion or implantation completely surrounding the gate (GATODE chip B).

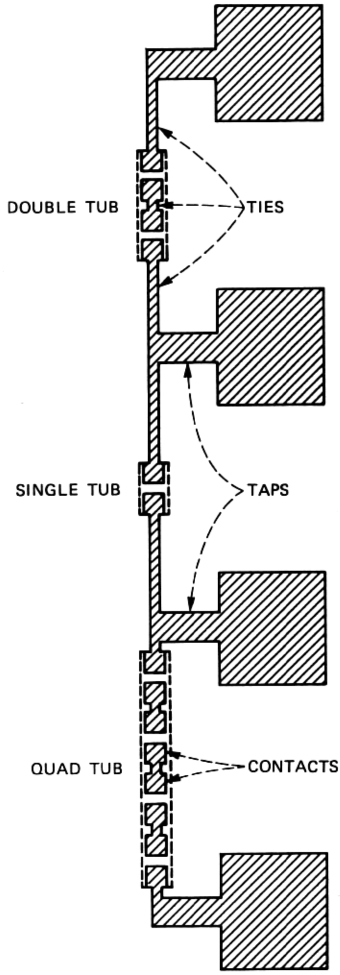


Fig. 11—Tapped string for the metallization test chip (METEST chip D).

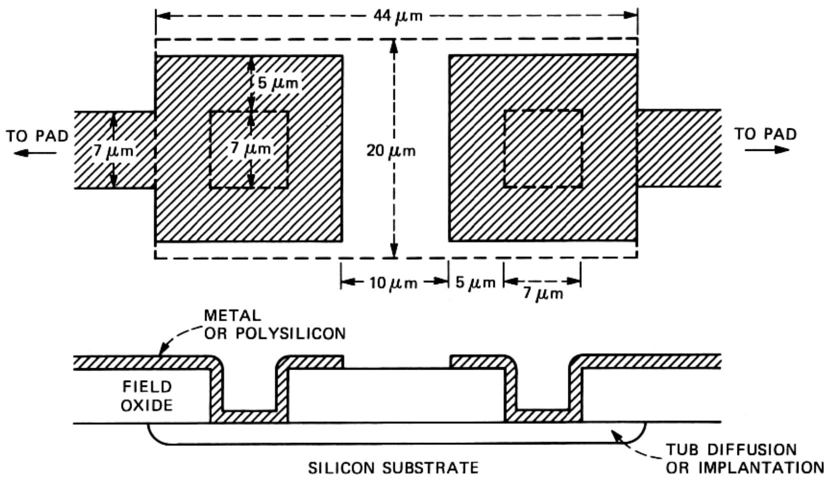
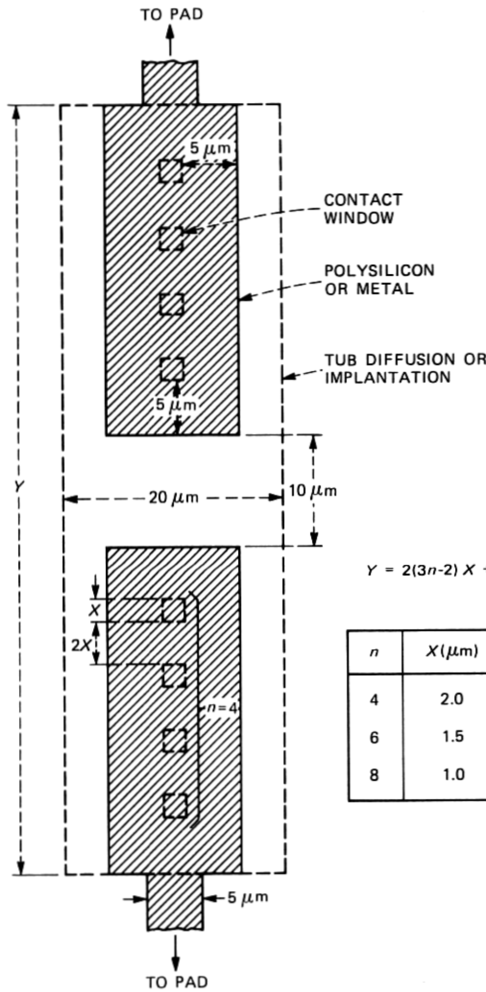


Fig. 12—Dual contact cell for the metallization test chip (METEST chip D).



$$Y = 2(3n-2)X + 30$$

n	X (μm)	Y (μm)
4	2.0	70
6	1.5	78
8	1.0	74

Fig. 13—Multiple contact cell for the metallization test chip (METEST chip D).

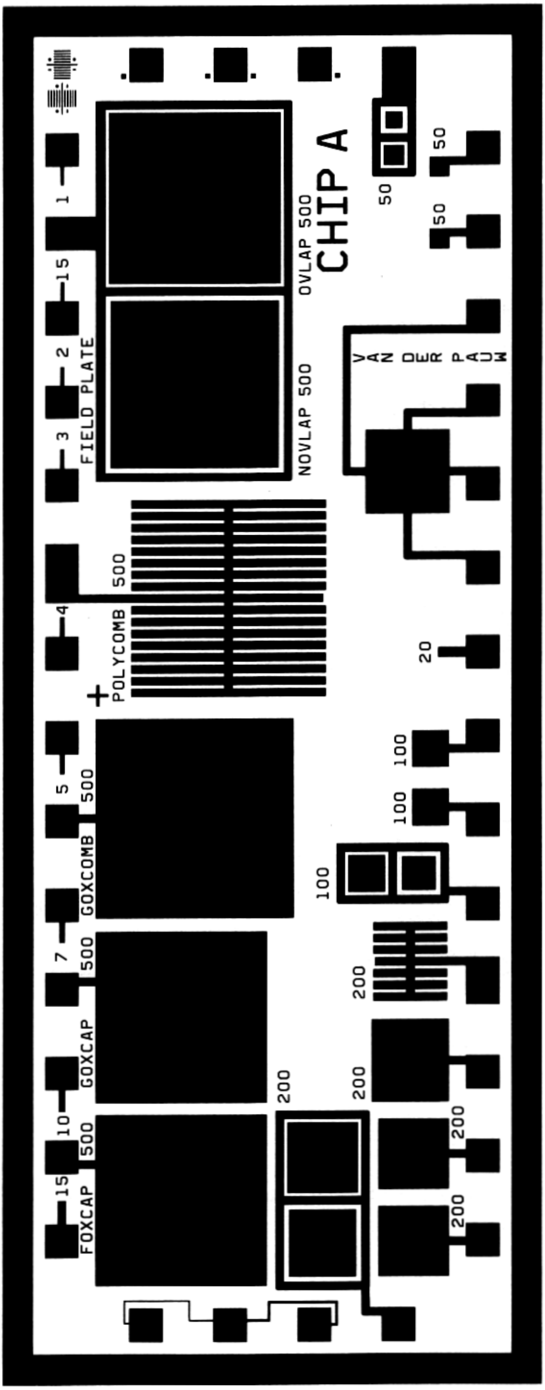


Fig. 14—Composite POLY and WINDOW levels for the A chip.

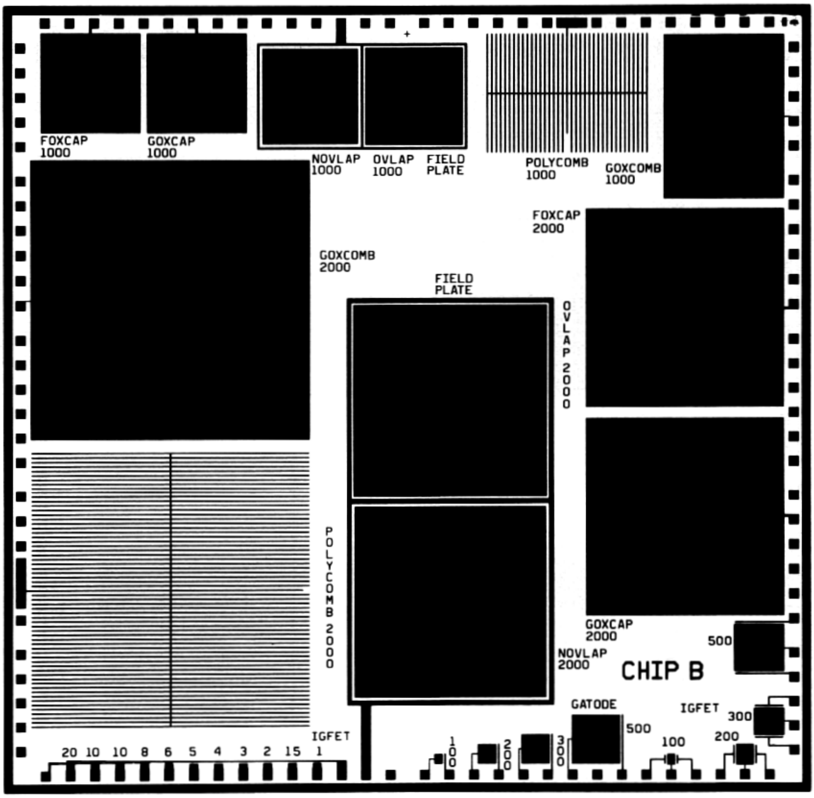


Fig. 15—Composite POLY, WINDOW, and METAL levels for the B chip. Some of the detail has been enlarged 3X to achieve adequate resolution for this illustration.

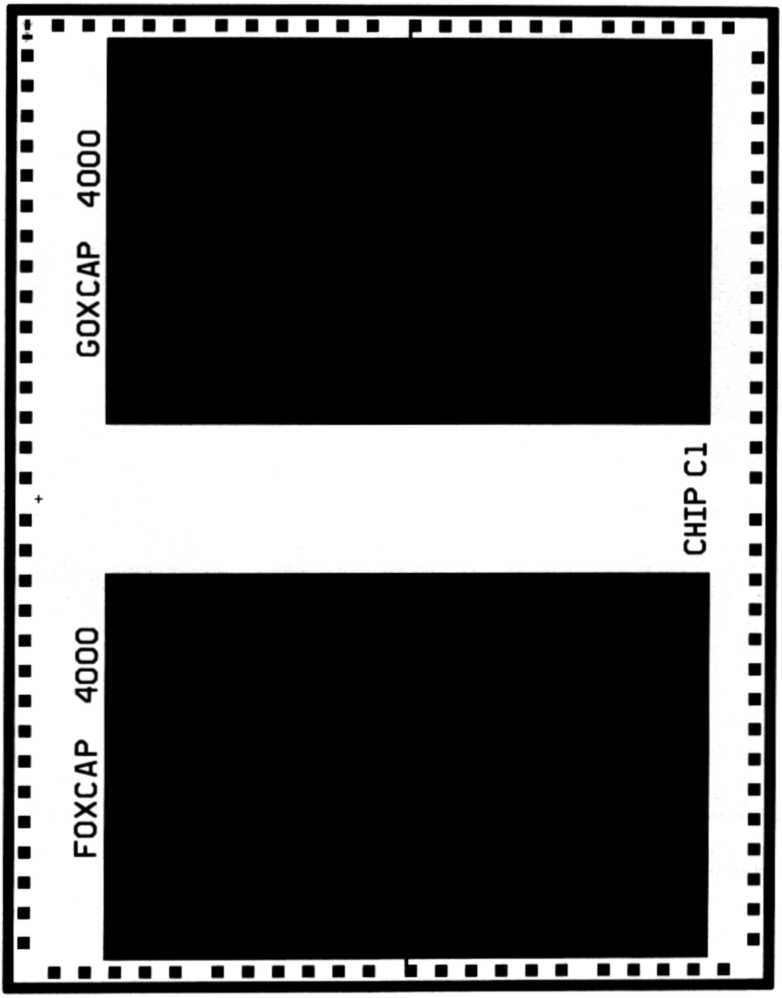


Fig. 16—Composite POLY and WINDOW levels for the C1 chip.

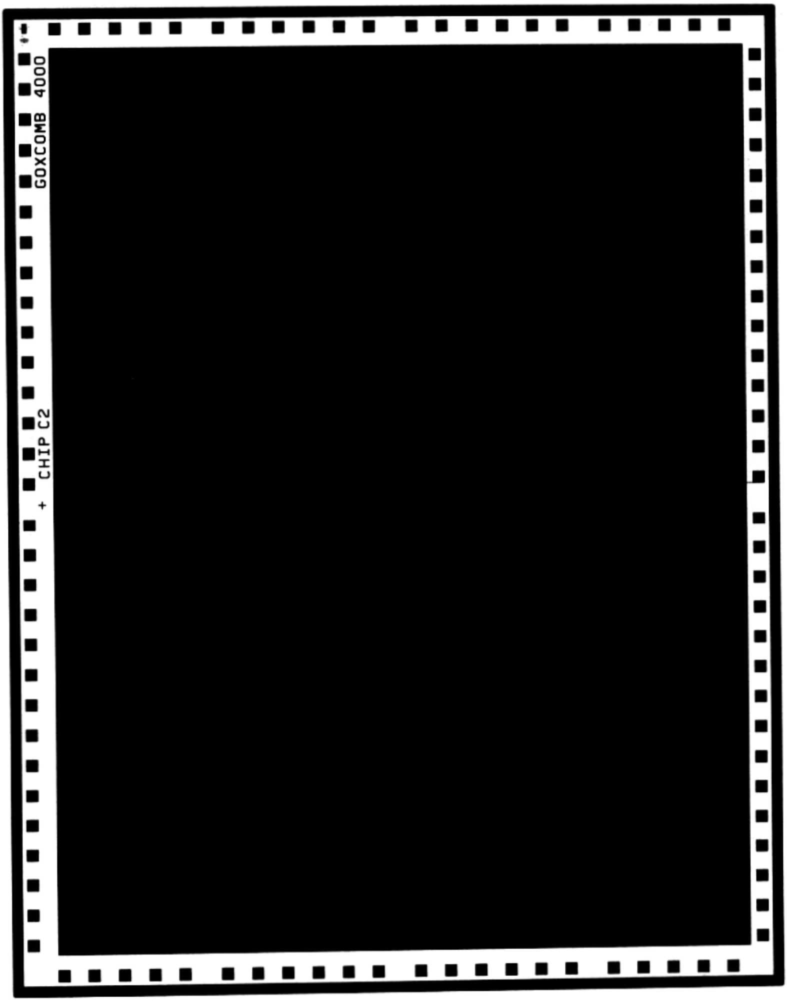


Fig. 17—Composite POLY and WINDOW levels for the C2 chip.

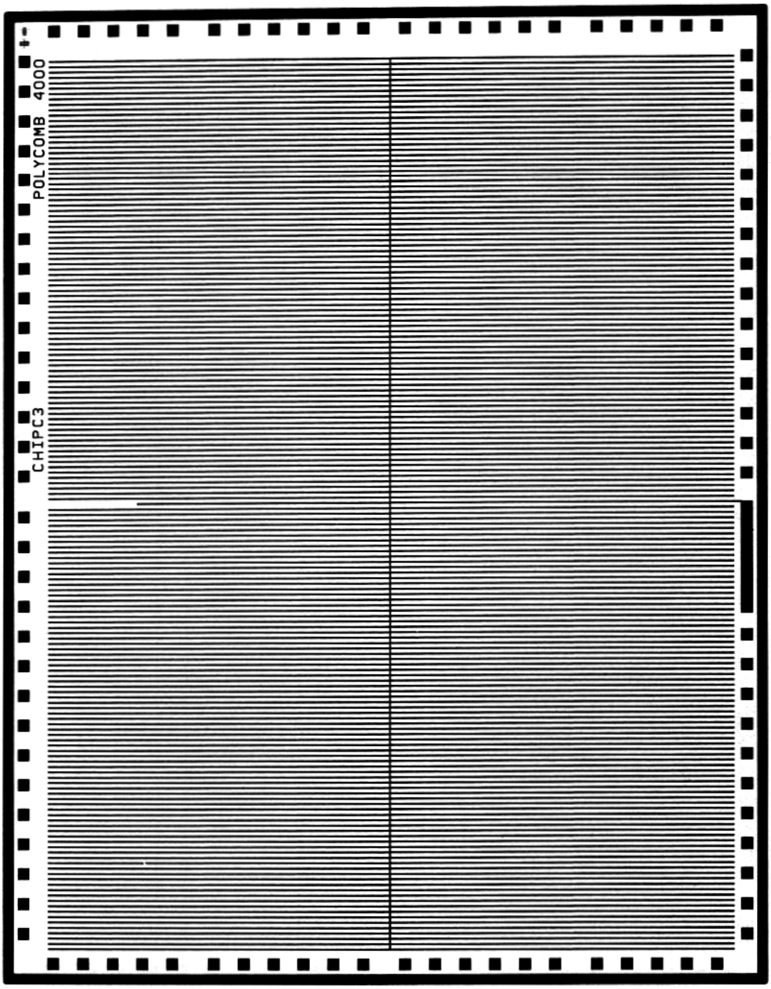


Fig. 18—Composite POLY and WINDOW levels for the C3 chip. Detail has been enlarged 3X to achieve adequate resolution for this illustration.

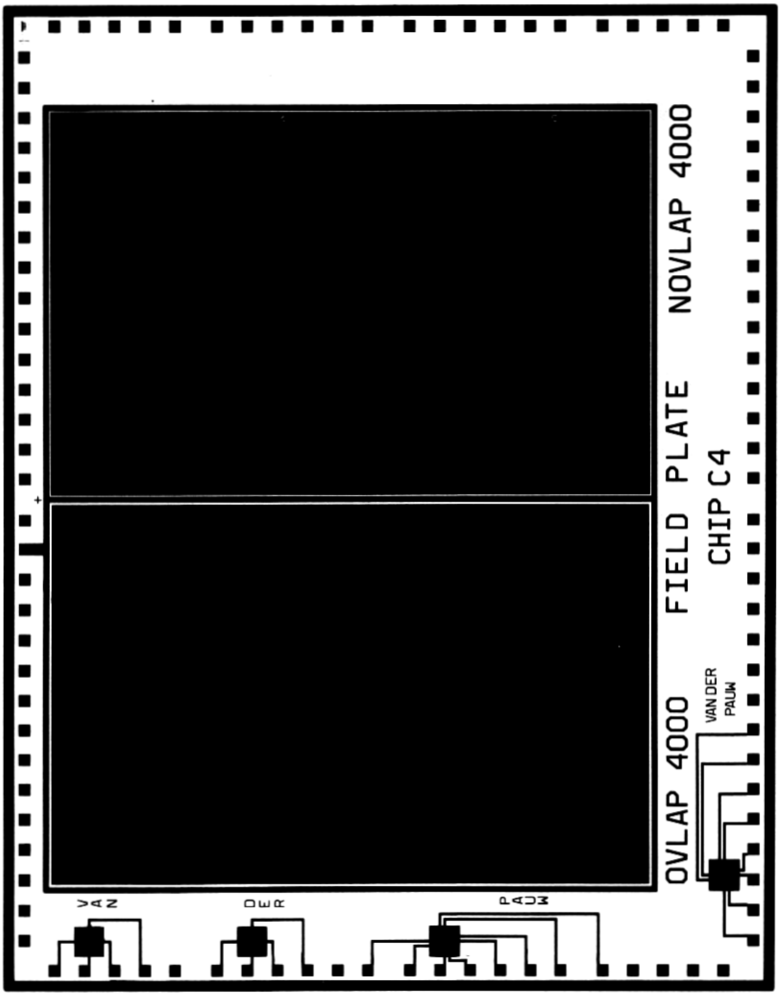


Fig. 19—Composite GUARDRING, GASAD, POLY, and WINDOW levels for the C4 chip. The frames surrounding OVLAP and NOVLAP have been enlarged 3X to achieve adequate resolution for this illustration.

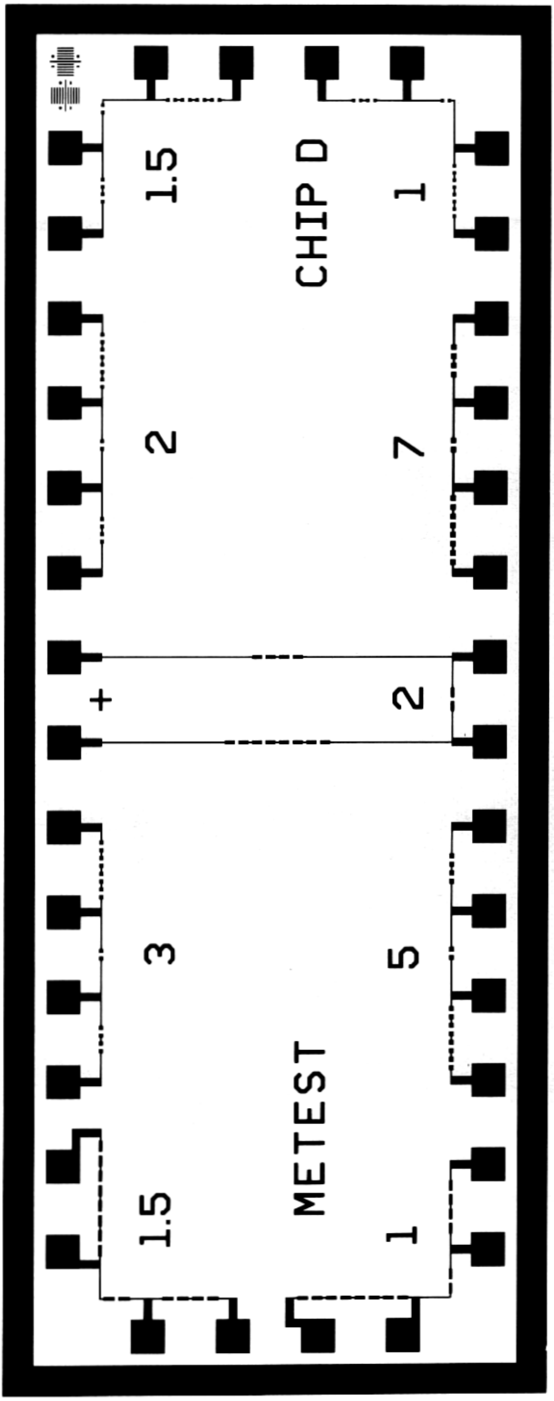


Fig. 20—Composite POLY and WINDOW levels for the D chip.

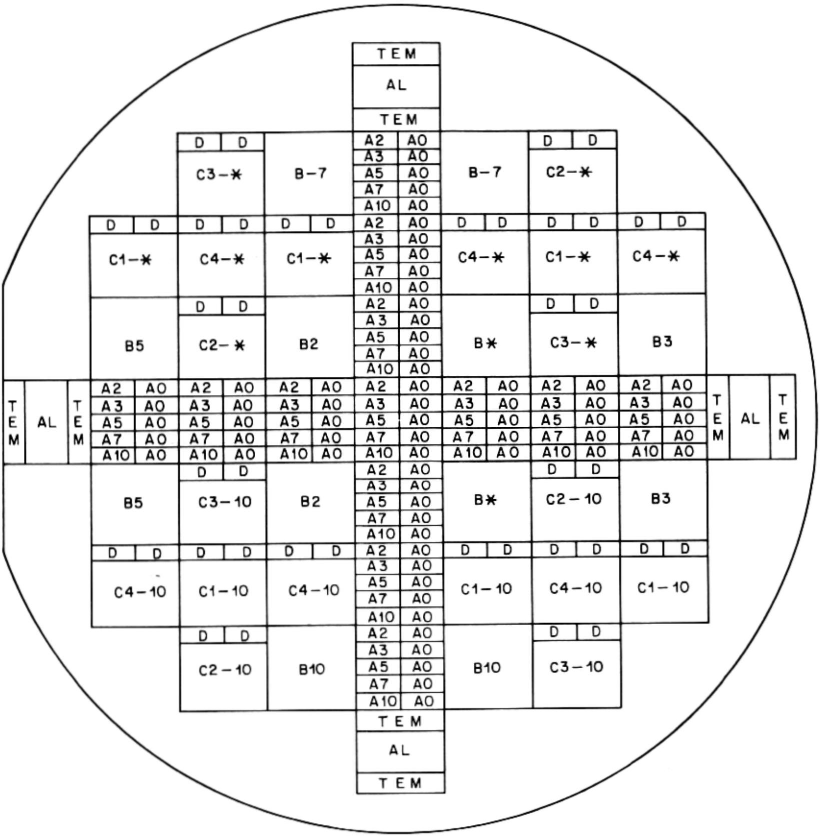


Fig. 21—Chip layout on the fine-line process development wafer.

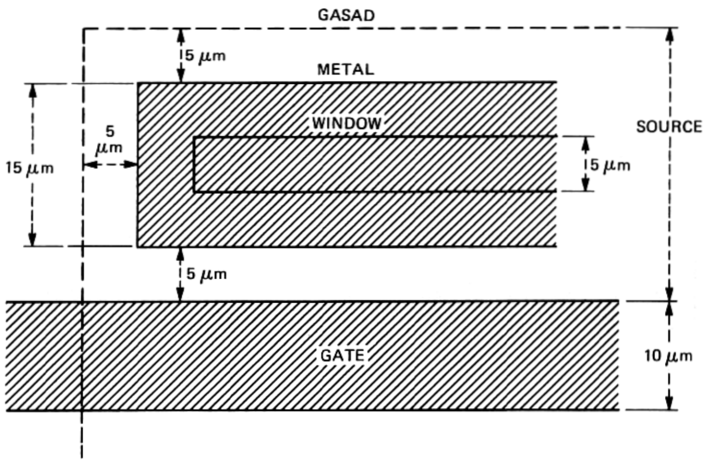


Fig. 22—IGFET design rules for fine-line process development system.

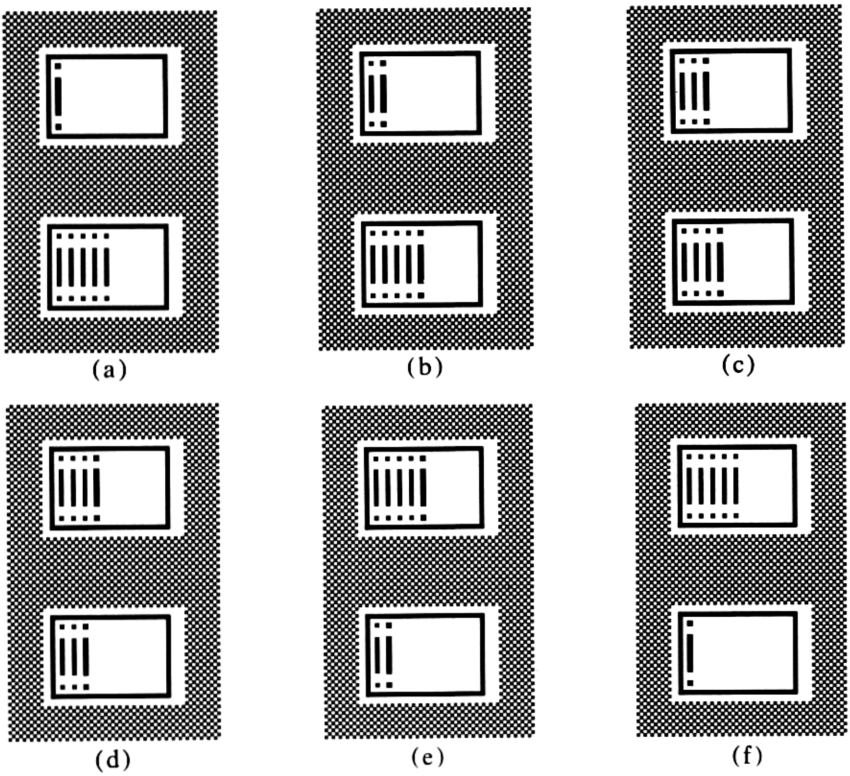


Fig. 23—MOPEP alignment features. (a) GUARDRING level. (b) GASAD level. (c) POLYCON level. (d) POLY level. (e) WINDOW level. (f) METAL level.

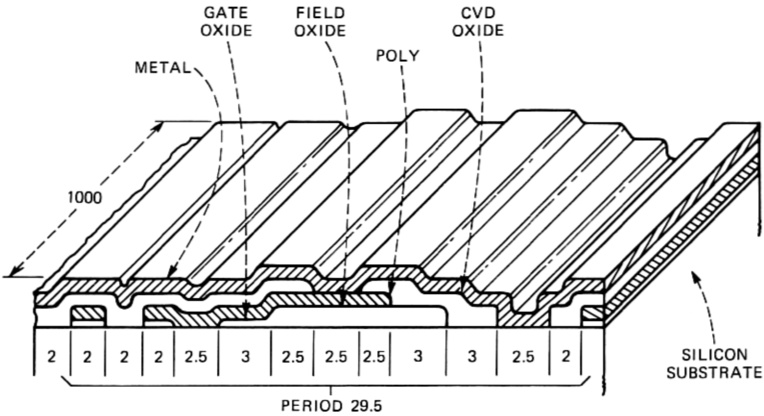


Fig. 24—TEM test chip.

GLOSSARY

CHANSTOP	channel stopping implantation or diffusion to avoid inversion of the silicon surface at the Si-SiO_2 interface
C-V	capacitance measured as a function of voltage
FOXCAP	field oxide capacitor
GASAD	gate and source and drain feature delineated in the field oxide prior to gate oxidation. Also, the second photolithographic level in the set of fine-line process development masks.
GATODE	gated diode, essentially an IGFET (see below) with common source and drain.
GOXCAP	gate oxide capacitor
GOXCOMB	a gate oxide feature with a comb-shaped structure
GUARDRING	electrically guarded structure, fabricated by ion implantation or diffusion, which straddles and surrounds the boundary of a metallization feature, forming a closed ring.
HEXCAP	six-fold or hexadic capacitor group
IGFET	insulated gate field-effect transistor
LSI	large-scale integration
METAL	metallization pattern, the final photolithographic level in the set of fine-line process development masks.
METEST	metallization test structure consisting of tapped strings with contacts to underlying diffused tubs.
MOPEP	modified Perkin Elmer projection alignment features
MOS	metal-oxide-semiconductor sandwich structure used

	for electrical characterization of device fabrication processes
NOVLAP	conductive pad not overlapping field oxide and forming the top level of a metal-oxide-semiconductor capacitor
OVLAP	conductive pad overlapping field oxide and forming the top level of a metal-oxide-semiconductor capacitor
PEP	Perkin Elmer projection alignment features
POLY	polycrystalline silicon which, when patterned, forms a conductive electrode for electrical tests. Also, an intermediate photolithographic mask level in the set of fine-line process development masks.
POLYCOMB	a polycrystalline silicon feature with a comb-shaped structure
POLYCON	polycrystalline contact to underlying silicon substrate. Also, an intermediate photolithographic mask level in the set of fine-line process development masks.
POLYSHEET	polycrystalline silicon feature for sheet resistance and linewidth loss measurements
SADSHEET	structure formed during gate and source and drain (GASAD) lithography to determine source and drain sheet resistance and linewidth loss
SEM	scanning electron microscope
TEM	transmission electron microscope
VANDER-PAUW	a symmetric structure introduced by L. J. van der Pauw[10] to determine the electrical resistivity of thin conductive layers
WINDOW	next to the last photolithographic mask level in the set of fine-line process development masks to form source and drain contacts to insulated gate field-effect transistors, junction contacts in gated diodes, and access to polycrystalline silicon features when the poly Si is covered by an intermediate dielectric.

REFERENCES

1. H. C. Poon and R. L. Johnston, unpublished work.
2. J. M. Andrews, J. Electron. Mater., *8* (1979), pp. 227–47.
3. R. A. Kushner, private communication.
4. D. M. Boulin, unpublished.
5. A. M. Mohsen and F. J. Morris, Solid-St. Electron., *18* (1975), pp. 407–16.
6. J. R. Brews and D. Kahng, unpublished work; U.S. Patent No. 4,135,289, applied for August 23, 1977, issued January 23, 1979.
7. B. V. Gokhale and J. Zeidenbergs, Technical Digest of the 1974 International Electron Devices Meeting. Abs. No. 23.1, p. 529.
8. G. W. Taylor, Solid-St. Electron., *19* (1976), pp. 495–503.
9. John Andrews, E. F. Labuda, and Paul Norton, The Electrochemical Society Extended Abstracts, Fall Meeting, Pittsburgh, PA, Oct. 15–20, 1978, Abstract 203, p. 543.

10. L. J. van der Pauw, Philips Res. Repts., *13* (1958), pp. 1–9.
11. B. R. Chawla, A. P. Gnadinger, and W. Rosenzweig, unpublished work.
12. R. F. Pierret, Solid-St. Electron., *17* (1974), pp. 1257–69.
13. P. L. Castro and B. E. Deal, J. Electrochem. Soc., *118* (1971), pp. 280–86.
14. D. J. Fitzgerald and A. S. Grove, Proc. IEEE, *54* (1966), pp. 1601–2.
15. E. H. Snow, A. S. Grove, and D. J. Fitzgerald, Proc. IEEE, *55* (1967), pp. 1168–85.
16. A. S. Grove and D. J. Fitzgerald, Solid-St. Electron., *9* (1966), pp. 783–806.
17. D. J. Fitzgerald and A. S. Grove, Surface Sci., *9* (1968), pp. 347–69.
18. G. W. Taylor, private communication.
19. J. R. Brews, private communication.
20. S. Vaidya, D. B. Fraser, and W. S. Lindenberger, J. Appl. Phys., *51* (1980), pp. 4475–82.
21. T. T. Sheng and R. B. Marcus, J. Electrochem. Soc., *127* (1980), pp. 737–43.
22. S. Vaidya, A. K. Sinha, and J. M. Andrews, J. Electrochem. Soc., *130* (1983), pp. 496–501.
23. J. M. Andrews, P. A. Heimann, and R. A. Kushner, Proc. First Int. Symp. on Very Large Scale Integration Science and Technology, Detroit, MI, October 17–21, 1982, Abstract 147, pp. 68–75.
24. C. J. Koeneke, S. M. Sze, R. M. Levine, and E. Kinsbron, IEDM Tech. Digest (1981), pp. 367–70.
25. P. A. Heimann, P. S. D. Lin, and T. T. Sheng, Electrochem. Soc. Extended Abstr., Fall Meeting, Detroit, MI, October 17–21, 1982, Abstract 195, pp. 309–10.
26. P. A. Heimann and J. E. Olsen, J. Appl. Phys. *53* (1982), pp. 546–9.